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Notice to Authors: Address all papers and editorial correspondence to R. E. Meagher, 168 Engineering Research Laboratory, University of Illinois, Urbana, Ill. To avoid delay, 3 copies of papers and figures should be submitted, together with the originals of the figures which will be returned on request. All material will be returned if a paper is not accepted.

Where Should I Send My Manuscript?

Every person working in the computer field should attempt to publish the results of his work when he feels that they will be of interest to other persons. When the time comes for doing this the question which arises is: "Where should the manuscript be sent for publication?" Within the framework of the IRE there are two journals to be considered: the PROCEEDINGS and the TRANSACTIONS ON ELECTRONIC COMPUTERS. Other journals may also be considered. Because papers must be read and considered by each separate journal, time will be saved if the author chooses the proper journal for his manuscript to begin with. This is written to discuss the types of papers suitable for the TRANSACTIONS ON ELECTRONIC COMPUTERS and the PROCEEDINGS.

The TRANSACTIONS ON ELECTRONIC COMPUTERS publishes papers which are (1) original and worthwhile contributions to the engineering aspects of electronic computers, and (2) of particular "timely" interest because of their importance to the many members in the computer field. In the second group are included articles of a review or tutorial nature which are timely in that many computer engineers will be interested, although the articles may not be new contributions. Each contribution is reviewed by three readers selected because of their competence in the subject of the article, and any comments or suggestions for improving the paper are passed on to the author. If the three readers recommend publication, the manuscript is considered by the Editorial Board which makes the final publication decision. Short notes or letters are published under "Correspondence" and do not receive the careful reviewing required for papers or articles. The TRANSACTIONS publishes material for specialists in the computer field.

The PROCEEDINGS will publish papers in the computer field if they are considered to be of general interest to the members of the IRE and if they represent a contribution of permanent value or great current interest. Thus publication in PROCEEDINGS requires a paper be of interest to readers with broader interests than computer engineers.

Papers which are sent to the PROCEEDINGS are considered by the reviewers for that journal. If a paper sent to the PROCEEDINGS is found to be of interest to the members of the Professional Group on Electronic Computers, but not of general interest outside of this group, then the paper is forwarded to the TRANSACTIONS ON ELECTRONIC COMPUTERS but, of course, it arrives one or more months later than it would have if it were sent directly. Conversely, papers sent to the TRANSACTIONS ON ELECTRONIC COMPUTERS are recommended for the PROCEEDINGS, if this seems appropriate. Papers will not, except under extraordinary circumstances, be published in both journals.

Papers are considered for the TRANSACTIONS ON ELECTRONICS COMPUTERS if they are of interest to the computer engineering profession. Therefore, papers on the use of computers which do not have a bearing on their design are usually not considered appropriate. Occasionally a paper appears which indicates an entirely new trend in the application of computers which should be brought to the attention of computer engineers by publication in the TRANSACTIONS. Papers in both the analog and the digital divisions of the computer field are equally valuable.

—The Editor

Constitution for IRE Professional Group on Electronic Computers*

This revised PGEC Constitution has been prepared by the PGEC Constitution and Bylaws Committee with Darrin H. Gridley as Chairman. It has been approved by the PGEC Administrative Committee, by the IRE Professional Groups Committee, and finally by the IRE Executive Committee at its meeting June 7, 1955. Mr. Gridley wishes to express thanks to all PGEC Administrative Committee members, both past and present, who have aided in the revision of this constitution.

The PGEC Bylaws follow the Constitution and contain additional information about the organization and operation of your Professional Group on Electronic Computers.

Article I

Name and Object

Section 1. This organization shall be known as the Professional Group on Electronic Computers of the Institute of Radio Engineers, Inc. (IRE).

Section 2. Its objects shall be scientific, literary, and educational, in character. The Group shall strive for the advancement of the theory and practice of computer engineering and of the allied arts and sciences, and the maintenance of a high professional standing among its members, all in consonance with the Constitution and By-Laws of the IRE and with special attention to such aims within the field of interest of the Group as are hereinafter defined.

Section 3. The Group shall aid in promoting close cooperation and exchange of technical information among its members and to this end shall hold meetings for the presentation of papers and their discussion, and through its committees shall study and provide for the needs of its members.

Article II

Membership

Section 1. The membership of this Group shall be limited to members of the IRE of any grade, including student.

Article III

Field of Interest

Section 1. The Field of Interest of the Group shall be that which stems from electronic computers, and shall include scientific, technical, industrial, or other activities that contribute to this field, or utilize the techniques or products of this field; subject, as the art develops, to additions, subtractions, or other modifications directed or approved by the IRE Committee on Professional Groups.

Section 2. The Field of Interest of the Group may be enlarged, reduced, or shifted moderately as the needs of the occasion indicate, with the provision, however, that if it overlaps the field of interest of another group to the extent that interference occurs, the IRE Committee on Professional Groups may draw up more exact lines of demarcation, and that if some other group wishes to enlarge their field to the disadvantage of this Group, that this Group will reasonably and in good faith consider the proposals and abide by any decision of the IRE Committee on Professional Groups.

Section 3. A subgroup may be formed and operated on any plan not inconsistent with the powers of the Administrative Committee of this Group.

"A sub-group formed in a Section shall be known as a Chapter. A Chapter may assist the Administrative Committee of this Group in the management of a National Meeting or Symposium promoted by this Group in a Section. The Chapter shall be responsible for coordination with the Section on such National Meetings or Symposia. A Chapter may promote Meetings of the section in the field of interest of this Group under the control and supervision of the Officers of the Section in which the Chapter is located."

Article IV

Financial Support

Section 1. The Group may not charge dues.

Section 2. The Group may make registration charges at its Group meetings, Conferences, Conventions, etc. The registration fee for non-IRE people may be higher than for IRE members.

Section 3. The Group may not make registration charges at a meeting, conference, or convention which it operates as part of a Sectional, Regional, or National meeting, conference, or convention.

Section 4. The Group may make assessments on its members for publication and additional purposes, but failure of a Group member to pay an assessment will not render him liable to dismissal from IRE membership.

Section 5. The Group may raise revenue by other means, such as advertising, shows, requests for contributions, etc. provided such means do not conflict with policies and revenue means of the IRE office, or encroach on revenue fields of prior established groups

* As amended, April 18, 1955. Approved, June 7, 1955.

or sections. The Group must receive from the IRE Executive Secretary an opinion that a proposed method of raising revenue is nonconflicting and not against IRE policy before embarking on the proposed plans.

Section 6. The Group may, but only after approval of the IRE Executive Committee, make a charge for sending out notices to non-group members to cover the extra expense thereby involved.

Section 7. Administrative Committee approval is required for all means of raising revenue.

Article V

Management and Officers

Section 1. The Group shall be managed by an Administrative Committee composed of a maximum of 15 members of the Group.

Section 2. The terms of office for Administrative Committee members shall be for three years, with the exception of a person who serves as Chairman PGEC during his third year on the Administrative Committee, in which case this person shall serve for four years. Five new members shall be elected each year.

Section 3. The Administrative Committee should annually elect one of its members as Chairman, and another as Vice-Chairman, whose terms shall be for one year. A Secretary-Treasurer should also be appointed annually for a one-year term, which officer need not be a member of the Administrative Committee.

Section 4. The Chairman, under direction of the Administrative Committee, shall have general supervision of the affairs of the Group. He shall preside at meetings of the Administrative Committee, at general meetings of the Group, and at the "Annual Meeting of the Group," and have such other powers and perform such other duties as may be provided in the Group By-Laws, or as may be delegated to him by vote of the Group Administrative Committee. In his absence or incapacity his duties shall be performed by the Vice-Chairman.

Section 5. The Vice-Chairman, under the direction of the Administrative Committee, shall assume the duties of the Chairman during the latter's absence or incapacity, and shall assume any duties of the office of Chairman when so directed by the Chairman. He shall have such powers and perform such duties as may be provided in the Group By-Laws, or as may be delegated to him by vote of the Administrative Committee.

Section 6. The Administrative Committee may utilize the services of IRE as bursar, in which case funds will be handled under rules established by the IRE Executive Secretary. He shall make only such disbursements as shall be ordered by the Administrative Committee.

Section 7. The Secretary-Treasurer shall be responsible for sending out notices according to plans delineated by the Administrative Committee or laid down in the Group By-Laws; he shall prepare the agenda for and record the minutes of all meetings of the Administrative Committee and general meetings of the Group; and he shall make such reports of his activities as may be required by the Administrative Committee, the IRE Committee on Professional Groups, or the IRE By-Laws.

Section 8. The Chairman, as soon as expedient after election, shall appoint the standing committees provided by the By-Laws.

Other Committees may be authorized by vote of the Administrative Committee and shall be appointed by the Chairman.

Members appointed shall serve until their successors are appointed or the committee dissolved.

Section 9. The Chairman, as an ex-officio member of the IRE Committee on Professional Groups, when notified of a meeting of said committee, is entitled to represent the Group at such meeting in person, by appointed delegate, or by letter.

Section 10. Newly elected Chairman, Vice-Chairman and members of the Administrative Committee shall assume office on the first day of the month following the day on which the National Convention of the IRE is held, unless a different time is provided by the By-Laws.

Section 11. No Professional Group or any officer or representative thereof shall have any authority to contract debts for, pledge the credit of, or in any way bind the IRE.

Article VI

Selection of Administrative Committee

Section 1. Election of the members of the Administrative Committee shall be by a method detailed in the By-Laws, which method shall include a suitable provision for additional nominations by other Group members than members of the Administrative Committee. This method shall be such that the membership of the Administrative Committee will reflect the national character of the Group. The names of such elected members shall be transmitted to the Chairman of the IRE Committee on Professional Groups and unless disapproval of such elected members is received within 60 days of such transmittal, the elections shall become final.

Section 2. Within-term vacancies on the Administrative Committee should be filled by appointments for the unexpired terms by the remainder of the Committee.

Article VII

Meetings

Section 1. The Group may hold meetings, conferences, symposia, or conventions either alone or in cooperation with Sections, Regions, National Convention Committees of the IRE, or other technical organizations, but the approval of IRE Headquarters must be obtained in advance in order to prevent conflicts of dates. The Group shall sponsor at least one technical meeting of national scope each year, which may be held during

the National Convention, or during some other IRE meeting, or as a separate conference.

Section 2. Meetings, Conferences, or Conventions of the Group shall be open on an equal basis to all members of the IRE. Separate Meetings, Conferences or Conventions of the Group shall not be held at a time or place which will conflict with a Sectional, Regional, or National Meeting, Conference, or Convention without approval of the Executive Committee of the IRE.

Since the aim of the IRE is to disseminate information, inclusion of sessions on governmentally classified material within the framework of IRE-sponsored Conferences and Symposia should, as a matter of principle, be avoided. However, it would be permissible for a classified meeting, sponsored by another organization, to be held in conjunction with an IRE conference, and for publicity on such a meeting to be included in the IRE mailing, so long as it is made perfectly clear that the classified meeting is not *sponsored* by the IRE.

Section 3. Meetings of the Administrative Committee shall be held at such times as are found necessary. Meetings of the Administrative Committee may be called by the Chairman of the Group at his own discretion, or upon request by two other members of the Committee.

Section 4. A majority of the members of the Administrative Committee shall constitute a quorum.

Section 5. A majority vote of the Administrative Committee shall be necessary in the conduct of its business except as otherwise provided in this Constitution. The voting power of a member of the Administrative Committee may be assigned to a proxy by written statement.

Section 6. Business of the Administrative Committee may be handled by correspondence, telephone, or telegraph where in the opinion of the Chairman matters requiring action can be adequately handled in that manner.

Article VIII

Amendments

Section 1. Amendments to this constitution may be initiated by petition submitted by twenty-five members of the group, or by the Administrative Committee, such petition being submitted to the Committee on Professional Groups and to the Executive Committee of the IRE for approval. After such approval has been secured, the proposed amendment shall be submitted by letter ballot to all members of the Group and approval of two-thirds of those voting shall be necessary for its enactment, provided, however, that not less than 20 per cent of the Group shall have voted, and that not less than 30 days shall have elapsed between the mailing of the voting ballots and the counting of the returned ballots.

Section 2. By-Laws of this Constitution may be adopted or changed by two-thirds vote of the Administrative Committee, provided that notice of the proposed change has been sent to each member of the Administrative Committee at least two weeks prior to such action. No By-Law shall take effect until a copy has been mailed to the Executive Secretary of the IRE.

Article IX

Publications

Section 1. Publication of any material may be entirely or partly by means of the Proceedings of the IRE by meeting its standards, and to the extent that is equitable to other fields of interest.

Section 2. Publication of any material may be by other means than the Proceedings of the IRE if the Group so desires, and is limited only by good taste and established policies of the IRE. The Group may make its own arrangements, or utilize the IRE's facilities in publishing. Publication shall be at the Group's risk and expense except when otherwise arranged with the IRE.

By-Laws

1. *Nominations Committee*—On or before December 1, each year, the Chairman shall appoint a Nominating Committee, which shall consist of a Chairman and four or more members of the Group. Two of the members of this committee shall be members of the Administrative Committee, these two members to be chosen from the group of five outgoing members.

2. *Nominations*—On or before January 1, the Nominations Committee shall submit for Administrative Committee approval a proposal for the geographical area to be represented by each of the five new members to be elected to the Administrative Committee. They shall be guided in this proposal by principles of efficiency and geographical distribution of members.

Where an approved area contains a Chapter, this Chapter shall be requested to select the new Administrative Committee member for that area; otherwise, the Nominations Committee shall submit two names for each area. The Nominations Committee may also submit two names for one member to be elected at large.

On or before February 20, the Nominations Committee shall submit to the Administrative Committee the names of the nominees for new Administrative Committee members. Also, the Nominations Committee shall submit the names of the proposed Chairman and Vice-Chairman, selected from the ten holdover members of the Administrative Committee.

Nominations by petition signed by 25 members of the Group will also be received by the Administrative Committee. Nominations are closed on February 20.

3. *Election Meeting.*—In March of each year the full Administrative Committee shall elect a Chairman and Vice-Chairman and, for each Administrative Committee position not to be filled by a Chapter, shall elect a first choice from among the nominees for that position. A plurality of votes shall elect. If an elected member declines the office, the second nominee will be chosen. Should both decline, the Nominations Committee shall select another name.

4. *The Chairman-Elect*—upon receiving notice of his

election as Chairman, shall immediately submit to the remainder of the newly elected Administrative Committee the name of a proposed Secretary-Treasurer for appointment. If a majority of the members of said Administrative Committee do not object within thirty days from date of oral submission or mailing said submission, the appointment shall become final. If a majority of the members of said Administrative Committee object a new name must be submitted. The incumbent Secretary-Treasurer shall remain in office until a successor is appointed and arranges to take over the office.

5. *The Administrative Committee* shall hold its annual meeting during the National Convention of the IRE.

6. *No meeting of the Administrative Committee* shall be held for the purpose of transacting business unless each member shall have been sent notice of the time and place of such meeting 20 days prior to the scheduled date of the meeting.

7. *The order of business* at the Annual Meeting of the Administrative Committee shall be:

1. Roll Call.
2. Reading of minutes of previous Annual Meeting.
3. Reading of report on business transacted other than at meeting.
4. Reading of Communications.
5. Report of Officers.
6. Report of Committees.
7. Unfinished business.
8. Elections to Administrative Committee for succeeding year, Chairman and Vice-Chairman.
9. New business.
10. Adjournment.

9. *Standing Committees*—The Chairman of the following standing committees shall be appointed by the Chairman as soon as possible after his election and such chairman shall hold office for one year coextensive with the term of office of the Chairman, except as otherwise noted in these By-Laws. The body of the Membership, Meetings, Publication, and Student Relations Committees shall be composed of whoever may be the Chairman of the corresponding Chapter committee; in those Chapters where the Committee Chairman declines to serve on the corresponding national committee, the Chapter Chairman will appoint another person to the National Committee. The body of the Sectional Activities Committee shall be composed of the Chapter Chairman. Additional members of any standing committee may be appointed at the discretion of the Committee Chairman.

1. Membership Committee.
2. Meetings Committee.
3. Publication Committee.
4. Sectional Activities Committee.
5. Student Relations Committee.
6. Awards Committee.

10. *Membership Committee*—The duties of the Membership Committee shall include encouraging membership in the Group of all members of the IRE who are interested in the field of interest to the Group.

The names of all applicants for membership in the Group shall be transmitted by the Secretary to the Membership Committee Chairman, and shall be recorded as members of the Group unless the Membership Committee shall within 19 days lodge with the Secretary information to the effect that the addition of such member is inimical to the best interests of the Group.

If and when the Group Constitution is amended to specify qualifications for membership, the Membership Committee shall pass upon applicants for Group Membership in the light of such qualifications.

The Membership Committee shall annually review the membership list of the Group to ascertain the names of those who appear to have ceased to be interested in the Group's field of interest, and shall recommend to the Administrative Committee the names of those individuals to be dropped from the membership list.

11. *Meetings Committee*—This Committee shall have the duty of promoting and managing meetings of the Group. It shall cooperate in arranging for participation of the Group at conventions and meetings.

The Meetings Committee shall take office and begin functioning immediately upon appointment and shall continue for one year plus such time as is necessary to bring to a termination all activities in connection with any meeting managed by said committee. Such an extension of the term of a Meeting Committee beyond the nominal year shall not preclude the appointment of the Committee at the designated time for the succeeding year.

12. *Publication Committee*—This Committee shall have the responsibility for the publication, on behalf of the Group, of technical journals, books, conference proceedings, newsletters, and such other material as may be authorized by the Administrative Committee, working in full cooperation with the Editorial Department of the IRE. It shall have the duty of securing material in the field of interest of the Group suitable for publication, of arranging for the review of technical material by competent reviewers, of editing the material, and of arranging for the printing of such material in accordance with standards accepted by the IRE. The Publication Committee may appoint editors and reviewers to carry out these functions. The Publication Committee shall also cooperate with the IRE in securing and reviewing material of interest to the Group for inclusion in the PROCEEDINGS OF THE IRE and other IRE publications. The expense of distributing Group publications to the Group's members shall be charged against assessments and other funds at the disposal of the Group.

The major technical publication of the Group shall be the IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, or the successor thereof. It shall be a serious technical journal in the field of interest of the Group. The Group's TRANSACTIONS ON ELECTRONIC COMPUTERS shall conform to the standards set for all IRE Professional Group Transactions.

13. *Sectional Activities Committee*—This committee is charged with promoting the organization of Section Committees of Group members in such sections as have a sufficient number of members as to justify an occasional Section Meeting in the field of interest of the Group. This committee is charged with carrying out this organization under the long established principle that meetings in any section come under the sole jurisdiction of the Section officers. This committee, therefore, may operate under any plan which does not violate the above principle such as:

(a) Inform the Chairman of a Section of the name of a member of the Group who is a member of said Section who is willing to assume responsibility in arranging a program for a Section meeting on a subject in the Group's field of interest to the satisfaction of the Section Program Committtee, or

(b) Appoint a committee of Group members in a Section to take the initiative in said Section to promote an occasional Section Meeting on a subject in the Group's field of interest, said tentative committee to be instructued to elect one of its members as a tentative Chairman, and to approach the Officers of said Section with the suggestion that their tentative Chairman or other member of the committee be appointed as a member of the Section Program Committee.

Upon securing Group representation on Section Program Committees, the Sectional Activities Committee shall annually arrange for the continuance thereof.

This Committee is charged with the preparation of an annual directory of National and Chapter Officers and Committee Chairmen.

This Committee shall also function as a communication link between the chapters and the Administrative Committee, serving to bring chapter activities and problems to the attention of the Administrative Committee and Administrative Committee actions to the attention of the chapters. Included in this function shall be such things as the preparation of the news column in the TRANSACTIONS ON ELECTRONIC COMPUTERS.

14. *Student Relations Committee*—The objective of the Student Relations Committee shall be to bring the IRE and, in particular, the Professional Group on Electronic Computers, to the attention of students in the various disciplines associated with electronic computing. Additionally, to hold that interest, it shall foster the provision of information on electronic computers to such students in connection with educational activities, professional meetings, professional advances, and new applications.

To aid it in its task, all communications concerning student interest and activities shall be directed to the Student Relations Committee. It shall advise the Membership Committee in connection with the qualifications required for student membership. Insofar as is possible, it shall work through the present chapter structure.

15. *Awards Committee*—This committee shall have the responsibility of administering the awards activities of the Group. Its duties shall include promotion of suitable Group awards and coordination of the awards activities of the other Group committees. It will be the duty of this committee to make selections of persons to receive Group awards or to delegate the responsibility for such selections to other committees or bodies where appropriate. It shall be the duty of this committee to maintain Group awards activities and policies consistent with the awards activities and policies of the IRE.

16. The Administrative Committee may circularize the membership regarding their continued interest in the Group and may drop from Group membership those that fail to give evidence of continued interest. The following list of actions shall be considered evidence of continued interest in the Group:

(a) Payment of any assessment within two prior years;

(b) Attendance at a Group Symposium within two prior years;

(c) Submitting a paper in the field of interest of the Group to the Group or to the IRE within three prior years;

(d) Giving adequate service on a Group Committee within three prior years;

(e) Giving talk, lecture, or notable discussion at a meeting of the Group at a National Convention or a Group Symposium, or Sectional Meeting in the Group's field of interest;

(f) Supplying other reason in reply to circularization that satifies the Group Administrative Committee.

The names of all members to be dropped from Group membership under this provision shall be reported to the Committee on Professional Groups with reasons therefore, and the names shall not be removed from the membership list for 30 days after such report to permit of a survey of said proposed action by the Chairman of the Committee on Professional Groups.

Any group member who is dropped from Group membership under this provision may appeal to the Committee on Professional Groups.

17. *Newly elected officers* shall assume office on the first day of the month following the date upon which the IRE National Convention is held, or as soon thereafter as can be conveniently arranged with retiring officers.

18. *The Secretary shall be responsible* for sending out notices of meetings. He may arrange with IRE Headquarters to handle their mailing, or make other arrangements agreeable to the Administrative Committee. If other facilities than IRE Headquarters are used, he shall be responsible for keeping the list of Group members from falling into unauthorized hands.

A Logical Reading System for Nonreturn-to-Zero Magnetic Recording*

A. S. HOAGLAND†

Summary—The nonreturn-to-zero method for the magnetic recording of binary information saturates the surface in a continuous fashion, one sense of saturation being used for a "1" and the opposite sense of saturation for a "0." A system is described for reading NRZ digital data which utilizes the inherent alternating characteristic of the readback signal waveform to effect a logical correction. The reading system corrects the "normal" sources of error which limit the usable bit storage density and set the degree of reliability. The system employs only amplitude sensitive waveform operators and samples the readback signal only at the regular clock times.

Introduction

THIS PAPER presents a method of reading magnetically recorded digital data which utilizes a logical decoding concept. The reading system to be described has been devised for the nonreturn-to-zero type of magnetic data recording. The NRZ (nonreturn-to-zero) mode of magnetic recording for digital data utilizes two opposite senses of surface saturation. Conventionally the surface is uniformly saturated in one direction for the binary digit "1" and in the opposite direction for a "0." Hence, the sense of saturation is reversed at each change in digit sequence. Readback essentially involves a derivative-type action,[1] and therefore an output voltage signal is associated with each change in the direction of saturation or the corresponding reversal in writing current (see Fig. 1). The reading

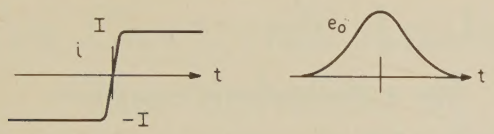

Fig. 1—Input-output response characteristic.

circuit incorporates a logical correction feature, based on the knowledge that the readback waveform has an inherent alternating characteristic. This circuit was developed for the drum memory of the California Digital Computer (Caldic) and has indicated an increased reliability and allowed the possibility of an increase in capacity.

Principle of Operation

Basically the reading system takes advantage of the following information contained in the signal waveform: successive signal peaks, corresponding to switching of the writing current, must alternate in sign. The circuit involves a one bit delay; i.e., the information normally available at bit time t_i is here available at t_{i+1}. The decoder examines the readback information at t_{i-1}, t_i, and t_{i+1} in deciding whether bit time t_i corresponds to a "1" or a "0."

Let the positive portion of the readback waveform be given the designator P and similarly let N apply to the negative portion. Thus, the P channel refers to the information path which responds to the positive portion of the input waveform. Then using the conventional strobing technique, which samples the signal once each bit interval, the following statements may be made.

No two successive strobes should be gated by either the P or N channel.

1. Adjacent strobes gated by the same channel must be differentiated, as only one can be correct.
2. An alternate strobe sequence gated by either channel indicates a strobe *should* have been gated by the opposite channel at the intervening clock time.

Normally, on reading, amplitude detection is used to form a pedestal throughout some interval of a signal peak; the strobes are clock pulses aligned with the signal peaks. Hence, the strobes are applied to a gate in conjunction with these pedestals to determine during each bit interval whether or not a signal was present. On this basis a brief discussion will follow of the difficulties that limit bit density and which the logical decoder is designed to overcome. The input signal may be considered either as rectified, in which case the gated strobes reverse a flip-flop monitoring the data, or separated into P and N channels, the gated strobe outputs being used as set and reset inputs to a flip-flop.

The output response for a step-like change in writing current has been indicated. Furthermore, for an arbitrary binary sequence the readback waveform can be anticipated by application of the principle of superposition. The clipping level used in sensing the pulse peaks must be chosen to allow reading of pattern variations as shown in Fig. 2. Hence, as the bit density is increased the following sources of error arise (see Fig. 2). Set and reset inputs are assumed.

Case 1. An isolated change in bit sequence. The readback waveform remains the same with increasing bit density, but separation between strobes will decrease. Eventually errors will occur as one or both adjacent strobes will be gated in addition to the desired one.

Case 2. A sequence of changes in the binary pattern. The increase in "overlapping" with higher bit density results in a reduction of the peaks as shown. Generally

* Original manuscript received, January 25, 1955; revised manuscript received April 9, 1955.

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[1] A. S. Hoagland, "Magnetic drum recording of digital data," *A.I.E.E. Transactions*, vol. 73, pp. 381–385; September, 1954.

a single change in the bit sequence will be "missed" first, causing a reading error.

Case 1 is usually the more important. The decoder corrects both these sources of error as any adjustment of the sensing level to avoid one increases the likelihood of the other.

The triggering ratio over which error-free reading occurs may be used as a criterion of reliability. This statement will be amplified later. Then errors of the type of Case 1 tend to limit the lower setting, and errors of the type of Case 2 the upper setting. For a given density the logical decoder increases the usable clipping ratio by extending both upper and lower limits, through corrections of errors indicated in Fig. 2.

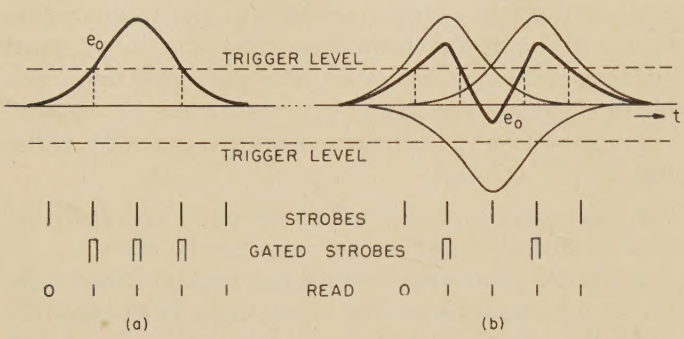

Fig. 2—Sources of readback error, (a) corresponds to the binary sequence 00111; (b) corresponds to the binary sequence 01011.

The circuitry for the correction of Case 1 errors involves an additional amplitude sensitive element, effecting a "zoning-type" action to more precisely locate the signal peak. The reception of two adjacent gated strobes, on either channel, must be resolved in favor of the one corresponding most closely to the signal peak, and this particular strobe may arbitrarily be either one of the two. This selection is accomplished by forming a gating pedestal at a higher amplitude on the incoming wave (see Fig. 3).

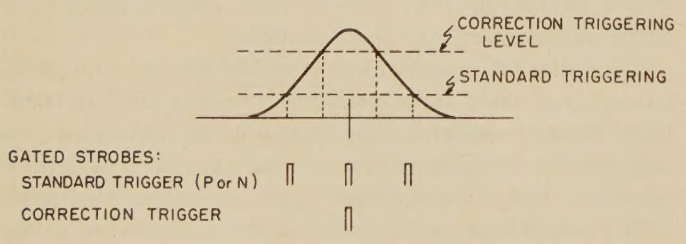

Fig. 3—Corrector trigger operation.

The only restriction placed on the correction level setting is that it isolate the desired strobe as shown. Considering the superposition concept, it is clear that these isolated signal peaks are the largest. It is immaterial whether or not this corrector trigger operates on signals received corresponding to a greater density of bit sequence changes. The addition of this sensing level allows the correct strobe to be identified in Case 1 and hence the circuit may logically interpret the signal information and correct this type of reading error.

The correction for missing a sequence change is entirely logical. If for example, the P channel reads a "1" at time t_{i-1} and no strobe is gated at read time t_i, then if the P channel again reads a "1" at t_{i+1} it is immediately known that t_i corresponds to a "0."

Logical Reading Circuit Description

The input signal is amplified and transmitted along three paths. One path is directly to a Schmitt trigger S-P. The negative portion of the input signal is inverted and operates another Schmitt, S-N. The third path is through a full-wave rectifier R to the corrector Schmitt S-C, set at the higher triggering level. T_1, T_2, and T_3 represent a three stage shifting register. Information read at strobe time is shifted from left to right (see circuit diagram, Fig. 4) at shift time, which is delayed relative to strobe time.

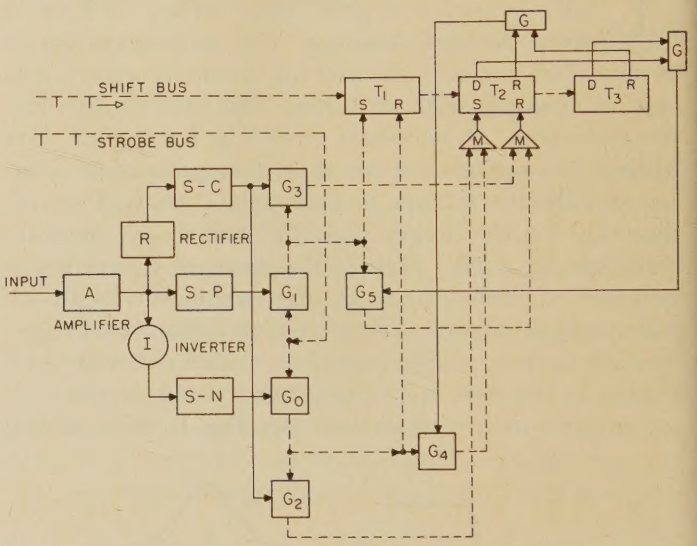

Fig. 4—Block diagram of logical decoder.

Normally when no correction is occurring the data strobes are gated through gates G_0 and G_1 to set (S) or reset (R) flip-flop T_1. The letter D on the flip-flop designates the high plate after the reception of a set pulse. Information read in T_1 at strobe time t_i is shifted into T_2 at shift time t_i. This information is shifted into T_3 at shift time t_{i+1}.

Flip-flop T_3 monitors the corrected readback data. The state of T_3 indicates the binary digit at the following bit period. The circuit operation to effect correction will be followed for each case considering the P channel active (Fig. 2).

Correction for the omission of a "0" (errors of the type of Case 2). Assume at time t_{i-1} a strobe was gated (a "1" read), setting T_1. Then, considering Case 2, no strobe is gated at t_i. Then just prior to strobe time t_{i+1} the state of the register is 111. Then pulse gate G_5 is open, controlled by a diode gate connected to the D plates of T_2 and T_3. The reception of a data pulse at t_{i+1} will alter the register, by resetting T_2, to read 101. The triangular symbol, designated M, represents a pulse

mixer. The insertion of this "0" in T_2 correctly inserts the "0" corresponding to strobe time t_i. The following discussion will make it clear that the operation of G_2 and G_3 can be ignored up to this point.

Correction for extra "1's" (errors of type 1). Consider the case where adjacent strobes on both sides of the correct one are gated by the P channel. This includes the reception of an adjacent pair as a special case. Assume the first strobe at time t_{i-1} has set T_1. After the associated shift time the register reads 110. At strobe time t_i both gates G_1 and G_3 are open. Hence while T_1 remains the same, T_2 is reset. Hence at shift time t_i the register reads 100 and after the shift, 110. Hence, bit time t_{i-1} is correctly interpreted as a "0." At strobe time t_{i+1} only gate G_1 is open and the register remains the same. At shift time t_{i+1}, T_3 is switched to the 1 state, indicating correctly the presence of a "1" corresponding to bit time t_i. The register then reads 111 and thus readout at time t_{i+2} will indiate correctly a one for bit time t_{i+1}.

It should be noted that the operation of G_2 and G_3 is not critical since logically every time T_1 is set, corresponding to the detection of a "1" on the P channel, T_2 should be in the 0 state. This merely corresponds to the fact that the input wave is alternating and each pulse should gate only one strobe, resulting as it does from a single writing current step.

If there exists some uncertainty in strobe timing with respect to the signal peaks, then S-C must be set to include at least this bit interval of the large signal peaks. However, the standard triggering level need not be raised, as would be the case were no logical correction included.

Normally the actual setting of the S-P and S-N triggering levels will be chosen to allow the greatest tolerance in signal amplitude about a nominal value. Such variations in signal strength will arise from changes in amplifier gain, head spacing, etc. This tolerance range is indicated by the operative triggering ratio on a standard signal. The justification for continuing to use only the triggering ratio of the S-P (or S-N) Schmitt as a measure for reliability or workable bit density with the decoder is the following. The setting of S-C is noncritical although the triggering level should properly be chosen with reference to the level of S-P (or S-N). Weaker signals may result in nonoperation of S-C, but this situation implies that the pedestal width of S-P and S-N is considerably reduced so that the correction feature is not required. Similarly, for signals larger than the nominal amplitude, S-C will always define the pulse peak more accurately than the other triggers.

The operation of this circuit will not introduce sources of error not formerly present as it does not use any modified form of the signal but retains amplitude sensitive detection. Further, it is capable of correcting errors, based not upon any more complicated sampling process, but rather logically, merely recognizing the inherent nature of the recorded signal. All logical information concerning the waveform is preserved, by utilizing P and N channels. A delay of one bit time is usually no handicap and the added complexity of the circuit is not great.

An Electronic Analog Computing Technique for the Solution of Trigonometric Problems*

A. S. ROBINSON†

Summary—**This paper describes a technique for the solution of trigonometric problems which utilizes a fixed carrier frequency, demodulators, modulators, resistors, condensers, and operational amplifiers in feedback configurations. Basic solutions are in the form of the amplitudes and phases of voltages relative to a reference carrier. A typical 400-cycle computer with an accuracy of 0.2 per cent is described in which output phases and amplitudes are expressed as the time delay between two pulses.**

Introduction

COMPUTATION based on a reference carrier frequency, with solutions in the form of the magnitudes and phases of voltages and currents relative to the carrier, is one of the oldest techniques in nonmechanical analog computation. The basic work in this field was directed toward the analysis of power distribution systems,[1] and has been extended to general purpose computations, including the solution of ordinary and partial differential equations.[2,3] Electric analog computers of this type use passive RLC elements and transformers to represent the linear terms of equations, as opposed to dc electronic differential analyzers, which use RC elements and operational amplifiers for this function.[4,5] The use of RC elements and operational

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[1] H. A. Travers and W. W. Packer, "An alternating-current calculating board," *Elec. Jour.*; vol. 27 pp. 266–270; May, 1930.

[2] E. L. Harder and G. D. McCann, "A large-scale general-purpose electric analog computer," *Trans. AIEE*, vol. 67, pp. 664–673; 1948.

[3] G. D. McCann, C. H. Wilts, and B. W. Locanth, "Electronic techniques applied to analog methods of computation," Proc. IRE, vol. 37, pp. 954–961; August, 1949.

[4] J. R. Ragazzini, R. H. Randall, and F. A. Russell, "Analysis of problems in dynamics by electric currents," Proc. IRE, vol. 37, pp. 444–452; May, 1947.

[5] C. A. Meneley and C. D. Morrill, "Application of electronic differential analyzers to engineering," Proc. IRE, vol. 41, pp. 1487–1496; October, 1953.

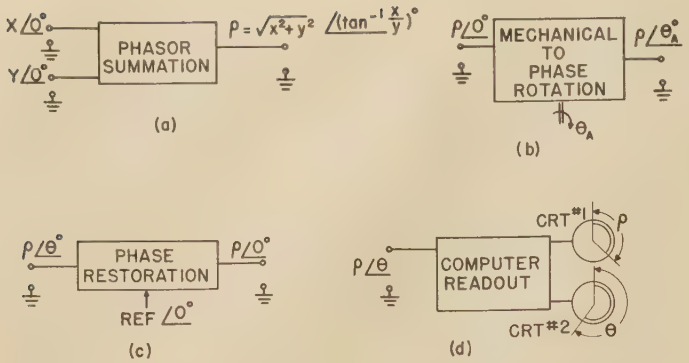

Fig. 1—Basic computer operations.

amplifiers for solving a right-angle triangle[6] and for precise wide-band measurement of phase[7] has been described in the literature. More recently, a special purpose computer based on the same principle has been constructed,[8] and a magnetic amplifier implementation of multiphase ac computing has been described.[9]

The technique to be described herein utilizes phasor[10] voltages as the analogs of space vectors in the solution of trigonometric problems. The magnitude of the phasor voltage is taken as the analog of the magnitude of the space vector and the phase of the phasor voltage relative to a reference carrier is taken as the analog of the angle of the space vector relative to a fixed space reference. Problem solutions are obtained by subjecting the phasor voltages to the same constraints as those imposed on the space vectors in the analogous physical problems. While this basic concept of computation is not new,[6–9] the technique described in this paper offers a new approach to the problem of imposing computing constraints. When this approach is used the "building blocks" required to synthesize a computer can be implemented utilizing relatively standard feedback amplifier techniques, so that it is feasible to place the major burden of accuracy on passive R and C elements. Relatively high accuracies can therefore be obtained in the individual building blocks, so that the over-all computer accuracy remains within reasonable bounds. In the application to be described the over-all computer was implemented with an accuracy of 0.2 per cent.

The trigonometric computations which can be performed using this technique are of particular interest in the solution of navigational problems involving wind corrections and in the solution of problems in fire control. They also are of interest in the field of function generation. Although problem solutions are obtained in the form of the phases and amplitudes of voltages,

[6] I. A. Greenwood, Jr., J. V. Holdam, Jr., and D. Macrae, Jr., "Electronic Instruments," MIT Rad. Lab., Cambridge, Mass., vol. 21, pp. 149–157; 1948.
[7] J. R. Ragazzini and L. A. Zadeh, "A wideband audio phasemeter," *Rev. Sci. Instr.*, vol. 21, pp. 145–148; February, 1950.
[8] J. R. Ragazzini and G. Reynolds, "The electronic complex plane scanner," *Rev. Sci. Instr.*, vol. 24, pp. 523–527; July, 1953.
[9] J. E. Richardson, "Analog computing with magnetic amplifiers using multiphase AC voltages," CONVENTION RECORD OF THE IRE, Part 7, pp. 30–33; 1953.
[10] A scalar quantity representing a sinusoidal voltage or current of given frequency, peak amplitude and phase.

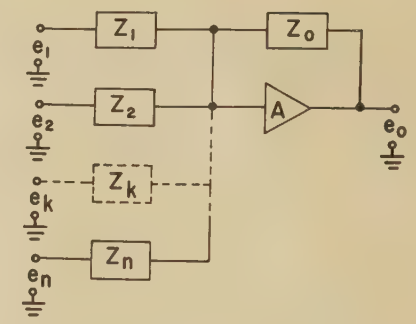

Fig. 2—General feedback amplifier configuration.

these quantities can easily be converted to time delayed pulses relative to zero crossover of the reference carrier. The time delayed pulses can then be used to convert the problem solutions to digital form, or they can be displayed in a variety of cathode-ray tube presentations.

Principles of Operation

The basic operations required to perform trigonometric computations are those of phasor summation, the conversion of mechanical rotation to phase rotation, the restoration of a voltage of arbitrary phase to phase zero, and the readout of problem solutions. These operations are tabulated in block form in Fig. 1. Phasor summation can be accomplished utilizing standard operational amplifier techniques. The output voltage of the amplifier shown in Fig. 2 can be derived as[4]

$$e_0 = -\sum_{k=1}^{n} e_k \frac{Z_0}{Z_k}\left[\frac{1}{1-\frac{1}{A}\left[1+\sum_{k=1}^{n}\frac{Z_0}{Z_k}\right]}\right]; \qquad (1)$$

which, for

$$\left|-\frac{1}{A}\left[1+\sum_{k=1}^{n}\frac{Z_0}{Z_k}\right]\right| \ll 1, \qquad (2)$$

reduces to

$$e_0 = -\sum_{k=1}^{n} e_k \frac{Z_0}{Z_k}. \qquad (3)$$

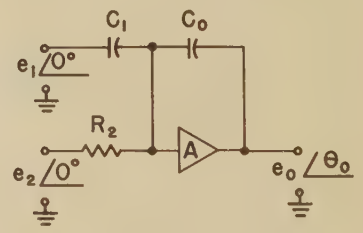

Fig. 3—Phasor feedback amplifier configuration.

For the configuration shown in Fig. 3, in which

$$Z_0 = \frac{1}{j\omega C_0}, \quad Z_1 = \frac{1}{j\omega C_1}, \quad \text{and} \quad Z_2 = R_2$$

$$e_0 = -\left[e_1\frac{C_1}{C_0} - je_2\frac{1}{\omega R_2 C_0}\right], \qquad (4)$$

and for operation at a carrier frequency f_c, with e_1 and e_2 in phase with the carrier and $\omega_C R_2 C_0 = 1$, $C_0 = C_1$,

$$e_0 \angle \theta_0 = -[e_1 \angle 0 - je_2 \angle 0]. \tag{5}$$

Evidently

$$|e_0| = \sqrt{|e_1|^2 + |e_2|^2} \tag{6}$$

and

$$\theta_0 = 180° - \tan^{-1}\frac{|e_2|}{|e_1|}. \tag{7}$$

If $e_1 \triangleq x$ and $e_2 \triangleq y$, the situation is as shown in Fig. 4. This approach leads to conventional power system notation in the sense of the phasor, since positive angles are measured counterclockwise from the positive x-axis.

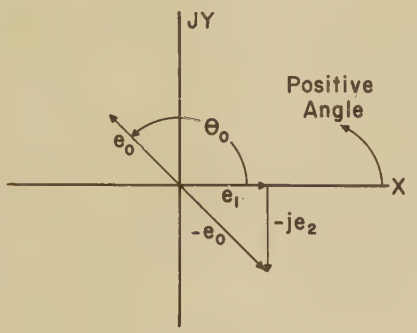

Fig. 4—Conventional phasor diagram.

In navigation applications it is often convenient, in order to place problems in one to one correspondence with map co-ordinates, to reverse conventional notation. In such cases $e_1 \triangleq y$ and $e_2 \triangleq x$. Positive angles are then measured clockwise from the positive y-axis and can correspond to magnetic headings if the y direction corresponds to magnetic north. This is shown in Fig. 5(a).

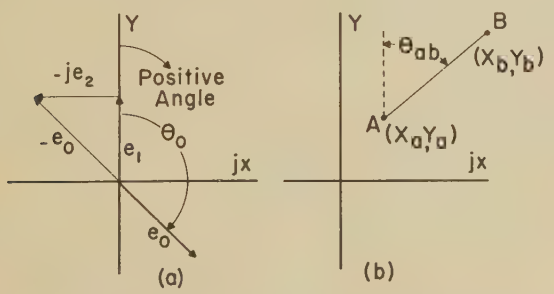

Fig. 5—Map co-ordinate phasor diagram.

As an illustration, the bearing and distance of point B in Fig. 5(b) from point A can be found by using any one of the circuits shown in Fig. 6. Selection of a circuit for a specific problem is governed by the required transient response, system noise, and available signs of variables. For convenience, only the circuit of Fig. 6(a) will be used later in describing typical applications of this computing technique.

The technique for summing a number of phasors using one amplifier is shown in Fig. 7. The indicated inputs are two positions (X_a, Y_a), (X_b, Y_b), one change in position $(\Delta X_{bc}, \Delta Y_{cd})$, and one distance and bearing $(\rho_{de} \angle \theta_{de})$. The limit to the number of inputs is fixed by the required accuracy of computation and (2).

A shaft rotation can be converted to a phase rotation with high accuracy by resolving a reference voltage into its X and Y components and performing a phasor addition on these components. This situation is shown in Fig. 8, p. 98, where rotation of the shaft θ_{de} will result in a rotation of output voltage phase through a corresponding angle, while output voltage magnitude will remain constant. In the implementation shown, the X and Y components are obtained with a resolver which utilizes a fixed auxilliary winding to provide the feedback reference voltage. The two component voltages are then added in a phasor addition, with each component given equal weight. The magnitude of the resultant output voltage is equal to that of the input voltage, while the phase of the output voltage is equal to the shaft angle θ_{de}. Referring back to Fig. 7, the dotted

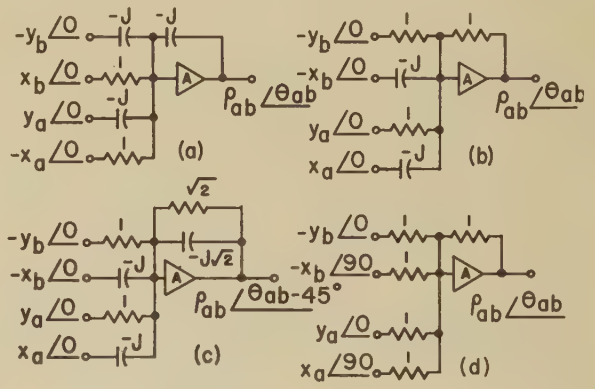

Fig. 6—Alternate forms of basic summing circuits.

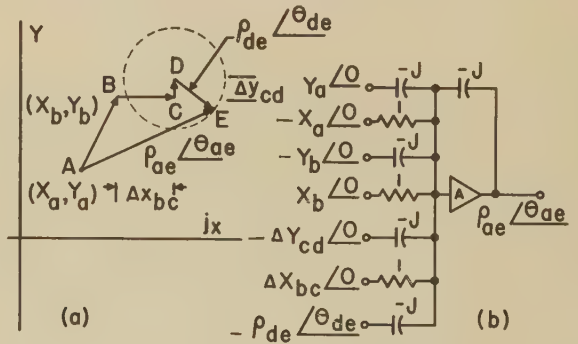

Fig. 7—Summation of a number of phasors.

circle is the locus of phasors obtained if $\rho_{de} \angle \theta_{de}$ of the figure is derived from a 360-degree rotation of the shaft in Fig. 8.

The function of the computing block designated "Phase Restoration" is to convert a voltage of arbitrary phase to phase zero without changing its magnitude. One simple implementation of this function is shown in Fig. 9. The feasibility of the phasor technique for a particular application will depend in many cases on the accuracy, simplicity and reliability of the circuitry used to implement the operation of phase restoration. In a particular application, it was found feasible

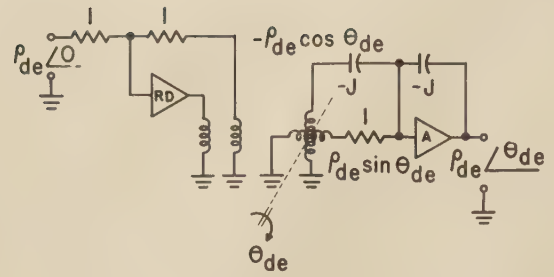

Fig. 8—Conversion of a shaft rotation to a phase rotation.

to obtain an accuracy of 0.13 per cent of full scale using the technique shown in Fig. 9. In achieving this accuracy it was found that the nonlinearities in simple LC filters could not be tolerated. Active filters composed of RC elements and operational amplifiers were therefore used for the filtering function.[11] The demodulator was nonphase-sensitive and used diodes in the feedback loop of an operational amplifier to achieve the required linearity. The modulator consisted of diode gating which converted the output of the demodulator to a square wave at the filter input. Although in all applications which will be discussed in this paper, the modulator reference is assumed to be fixed at zero phase, it is possible to derive the modulator reference from one of the quantities being computed, and thus to extend the versatility of the computing technique.

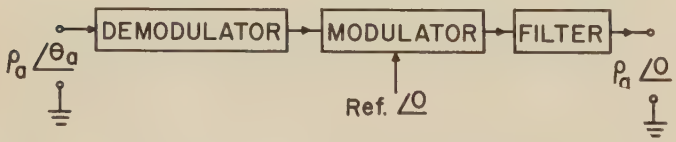

Fig. 9—Phase restorer implementation.

Since problem solutions appear as voltages shifted relative to the reference carrier, means are required to measure both amplitude and phase. A highly accurate procedure involves nulling the unknown voltage against reference and quadrature voltage supplies, thus determining the two components of the unknown. Phase and amplitude can then be computed. Although accuracies in the order of 0.01 per cent can be obtained in this manner the procedure is slow and inconvenient.

Fig. 10 shows the block diagram of a system in which both phase and amplitude of the output voltage can be read out directly at a rate equal to the carrier frequency. Each answer appears as an arc on a cathode-ray tube. The cathode-ray tube deflection voltages generate a Lissajou figure which is intensified at carrier reference zero and blanked with a time delayed pulse. The time delayed pulse is derived by marking zero crossover of the unknown voltage in the case of phase and by detecting the unknown voltage magnitude and comparing it to a standard sweep in the case of amplitude. If a digital readout is desired the same time-delayed pulses can be used to gate clock pulses into phase and amplitude counters. In like manner, many alternate forms of readout are feasible, including simple analog dc voltages or single line cathode-ray tube displays in which the magnitude of a line from the origin corresponds to phasor magnitude and the angle from the vertical corresponds to phasor phase.

[11] C. C. Shumard, "Design of high-pass, low-pass, and band pass filters using RC networks and direct current amplifiers with feedback," *RCA Rev.*, vol. 11, pp. 534–564; December, 1950.

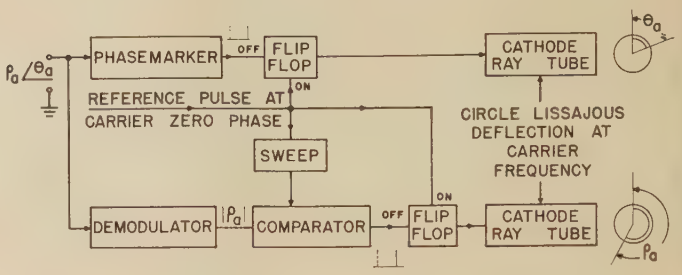

Fig. 10—Computer readout block diagram.

The process of computer synthesis involves the establishment of a computing loop composed of these components which is the analog of the vector problem under consideration. The process is best described by considering a typical application.

Applications

A representative application of a computer synthesized from these components is shown in Fig. 11. The positions (X_a, Y_a), (X_b, Y_b) and speeds (S_a, S_b) of points A and B are known, as is the direction of motion (θ_{b0}) of point B. Although positions and directions are derived in a fixed co-ordinate system it is known that all measured points are moving with a speed S_c and in a direction (θ_{c0}) relative to the fixed system. The problem is to find the required direction of motion (θ_{ac}) of point A to hit point B, and "time to go" (T) until this occurs.

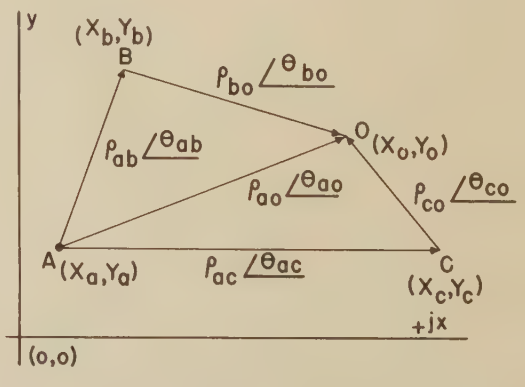

Fig. 11—Phasor diagram of a typical problem solution.

A block diagram of the problem solution is shown in Fig. 12. S_a, S_b, S_c, θ_{b0}, and θ_{c0} are introduced as shaft rotations.

For simplicity, let us first assume that S_c is zero, in which case the entire problem solution occurs within the dotted box of Fig. 12, and the corresponding prob-

em geometry is simply ABO of Fig. 11. The triangle o be solved is then

$$\rho_{a0}\,|\,\underline{\theta_{a0}} = \rho_{ab}\,|\,\underline{\theta_{ab}} + \rho_{b0}\,|\,\underline{\theta b_0}. \tag{8}$$

Now $\rho_{ab}|\underline{\theta_{ab}}$ is completely determined by (X_a, Y_a) and (X_b, Y_b). Also, θ_{b0} is a computer input. In order to form a computing loop an additional relationship is required between $|\rho_{a0}|$ and $|\rho_{b0}|$. The relationship is obtained from the problem statement, for in order for the two points to collide they must both take the same amount of time (T) to reach position 0. Then

$$|\,\rho_{b0}\,| = (S_b)(T_b), \tag{9}$$

$$|\,\rho_{a0}\,| = (S_a)(T_a) \tag{10}$$

and

$$T_b = T_a = \frac{|\,\rho_{b0}\,|}{S_b} = \frac{|\,\rho_{a0}\,|}{S_a}. \tag{11}$$

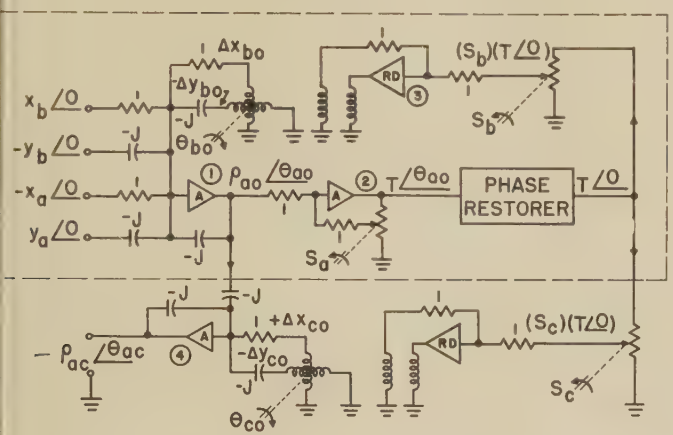

Fig. 12—Typical phasor computer block diagram.

Referring to Fig. 12, let us assume that $\rho_{a0}|\underline{\theta_{a0}}$ is available at the output of amplifier 1. At amplifier 2 this voltage is divided by S_a to obtain $T|\underline{\theta_{a0}}$. $T|\underline{\theta_{a0}}$ is then passed through a phase restorer and is multiplied by S_b at the S_b potentiometer. The voltage $(S_b)(T)|\underline{0^0}$ is then available at the input to amplifier 3. But from (9) this is simply $\rho_{b0}|\underline{0^0}$. All that now remains is to shift this voltage in phase by the angle θ_{b0} to obtain $\rho_{b0}|\underline{\theta_{b0}}$. At amplifier 1 $\rho_{b0}|\underline{\theta_{b0}}$ and $\rho_{ab}|\underline{\theta_{ab}}$ combine to form the problem solution, $\rho_{a0}|\underline{\theta_{a0}}$. But this is where we started, so that the voltage analog is complete.

If the effect of S_c is now included, points A and B will no longer collide at position 0, but rather at a new location, designated C. The new triangle to be solved is AOC, and the corresponding equation is

$$\rho_{ac}\,|\,\underline{\theta_{ac}} = \rho_{a0}\,|\underline{\theta_{a0}} - \rho_{c0}\,|\,\underline{\theta_{c0}}, \tag{12}$$

But

$$|\,\rho_{c0}\,| = (S_c)(T). \tag{13}$$

The equation is therefore closed at amplifier 4 by summing $\rho_{a0}|\underline{\theta_{a0}}$ and the voltage $-(S_c)T|\underline{0^0}$, shifted in phase by the angle θ_{c0}.

Impossible problems can be set into the computer (say $S_b > S_a$, $\theta_{b0} = \theta_{ab}$), in which case the circuits saturate. When a solvable problem is inserted the loop moves out of saturation to the correct solution automatically.

Another application of interest has been pointed out by Richardson[9] and arises due to the algebraic relations associated with certain geometric configurations. An

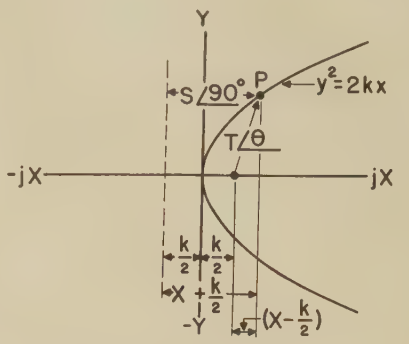

Fig. 13—Geometry of a parabola.

example is shown in Figs. 13 and 14, where the computer required to generate the parabola $y^2 = 2kx$ is shown. Referring to Fig. 13, by definition a point on a parabola obeys the stipulation that $|S| = |T|$. The computer shown in Fig. 14(a) determines the value of $2k$ which satisfies this constraint for given input voltages X and Y, and thus computes the value of Y^2/X. To trace the computing loop, assume that $T|\underline{\theta}$ is known. At the output of the phase restorer the voltage $T|\underline{0}$ is then available. But by definition $|T| = |S|$. Further, $(S-X) = k/2$, so that $k/2$ is available at the output of amplifier 2. But $y + j[x - (k/2)] = T|\underline{\theta}$, so that $T|\underline{\theta}$ can be computed at amplifier 1. Since the demodulator in the phase restorer is itself a feedback amplifier, a number of the

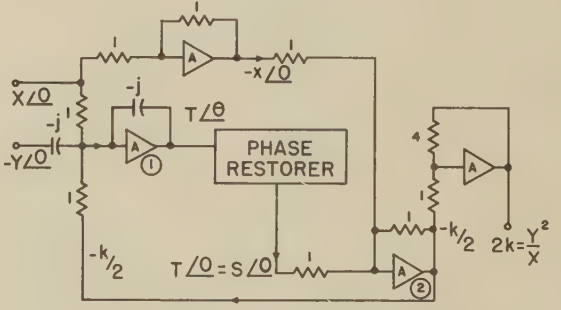

Fig. 14—Parabola implementation.

amplifiers shown in Fig. 14(a) are not really required. Fig. 14(b) shows a simplified version of the same computing loop. Richardson has pointed out that the equation of any conic section can be implemented using phasor techniques, since comparable geometric constraints are available.

Characteristic Circuitry

The techniques used to implement the blocks described above are relatively standard. In order to provide a measure of the accuracy and order of complexity of the implementations involved, the characteristics of the basic components for a 400-cps computing system will be briefly summarized.

A block diagram of a resolver driver has been shown in Fig. 8. Feedback is provided from an auxiliary winding on the resolver bearing a fixed space relationship to the primary winding. This technique represents a considerable improvement over implementations using direct drive of a resolver primary, since it includes the resolver in the feedback loop. Distortion and variability of transformation ratio which result when direct drive is used are effectively reduced by the loop gain in this implementation. One 2-tube implementation of this amplifier has a forward gain of approximately 77 db and output noise with the input grounded is less than .3 mv. Distortion is less than 0.05 per cent at the maximum output voltage of 60 volts rms. Over-all phase shift is not more than 0.06 degree for any output up to the maximum obtainable.

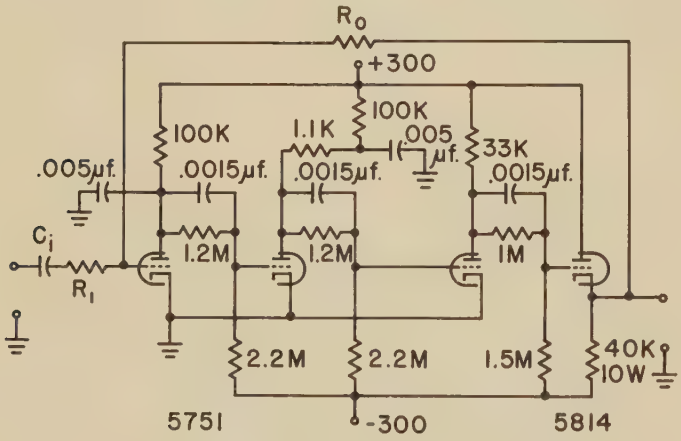

Fig. 15—Operational amplifier schematic diagram.

The schematic diagram of a typical operational amplifier is shown in Fig. 15. This unit can produce 30 volts rms across a $10K$ load and has a nominal forward gain of 80 db. Four inputs can be summed with unity gain while retaining a loop gain of 66 db. With stabilization as shown the transform of the amplifier gain is

$$A(s) = -2.1\times10^{6}\,\frac{(s+0.628\times10^{3})(s+188.4\times10^{3})}{(s+1.26\times10^{3})(s+6.28\times10^{3})^{2}}. \quad (14)$$

This form has proved to be convenient, since it permits the amplifier to be used in a number of other computing configurations while retaining adequate gain and phase margins. In all cases it is necessary to provide externally both dc and ac feedback paths. In the summing operations both paths are combined. An example of separate paths is the 90-degree phase shifting amplifier.

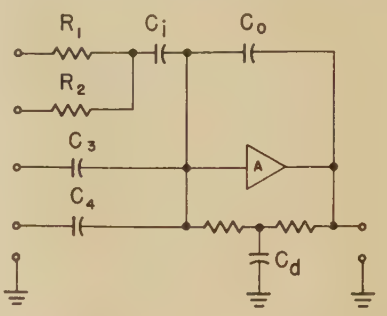

Fig. 16—90-degree phase shifting amplifier block diagram.

The 90-degree phase shifting amplifier uses the operational amplifier in a configuration as shown in Fig. 16. The capacitor C_d is chosen to make the contribution of this feedback path negligible at 400 cps. Since computing feedback occurs through C_0 only this circuit is equivalent to that of Fig. 6(a). The reactance of C_i is made negligible compared to the value of the input resistors. The rate of change of gain between amplifier output and the input to one of the resistors is plus 6 db per octave as frequency is decreased. Gain is therefore enhanced below 400 cps until frequencies are reached at which C_d and C_i take effect. If low-frequency noise is present in the system it will be amplified. This effect is eliminated and condenser C_d can be removed if the configuration of Fig. 6(c) is used. The undesirable feature of this approach is that the output phase is shifted 45 degrees from the true answer. The configuration of Fig. 6(b) results in a rate of change of gain between amplifier output and an input to one of the condensers which is plus 6 db per octave as frequency is increased. Gain is enhanced above 400 cps, and high-frequency noise in in the system will be amplified. If this approach is used the operational amplifier compensation networks must be changed. The configuration of Fig. 6(d) is straightforward and reliable, but requires that inputs of appropriate phase be available. In feedback computations it is usually convenient to derive both x and y at the same phase, so that the circuit of Fig. 6(d) cannot be used.

A typical nonphase sensitive demodulator uses an operational amplifier in a configuration as shown in Fig. 17. Feedback at 400 cps must occur through the diodes since the condenser C_d is chosen to make the contribution of its feedback path negligible at 400 cps. The accurately rectified half sinusoids are both filtered to give push-pull dc output. An output of 14 volts dc is obtained for a 30 volt rms input. Linearity of the unit is better than 0.05 per cent of full scale.

One type of phase restorer uses a nonphase-sensitive demodulator, a push-pull hard diode gate and a low pass filter consisting of operational amplifiers and RC ele-

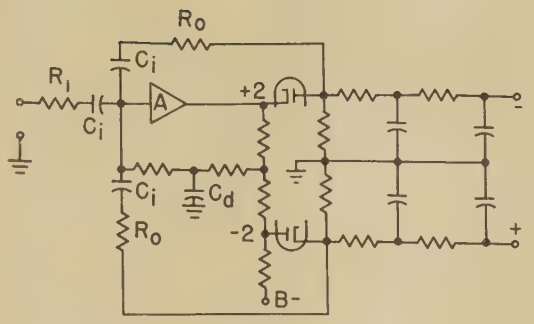

Fig. 17—Nonphase-sensitive demodulator block diagram.

ments. The low pass filter design is due to Shumard,[11] and was found necessary to overcome the nonlinearities of the inductors in LC filters. A typical phase restorer requiring push-pull square wave control voltages at 400 cps uses 3 tubes for the nonphase-sensitive demodulator, 5 tubes for the push-pull hard diode gate, and 4 tubes for two stages of filtering. The linearity of the 13 tube unit is 0.13 per cent of full scale.

In one form of phase marker an operational amplifier is used with diodes in the feedback loop, followed by additional amplification and a blocking oscillator. A 5-tube implementation marks zero crossover of input voltages between 0.3 and 50 volts rms with an accuracy of plus or minus 0.5 degree.

Conclusion

The technique described has been found practical for the solution of more complex trigonometric problems than have heretofore been considered with this approach. Its advantages lie in the use of circuitry that is relatively cheap, uncomplicated, light, and compact, with few moving parts and reasonable accuracy.

The components described here are not necessarily considered optimum, either in characteristics or implementation. They were designed for a particular application, and therefore do not exhibit all of the flexibility which might be appropriate for general purpose use of this technique. They do, however, represent a first step and give some definite answers concerning the order of accuracy and complexity associated with this type of computing system.

Acknowledgment

This work was performed as a subsidiary portion of a large control system problem. The computing philosophy is due to Professor J. R. Ragazzini. The over-all project was under the direction of Professor L. H. O'Neill and Mr. A. F. Sciorra. The work has been supported jointly by the Rome Air Development Center and the Air Force Cambridge Research Center.

An Analog Computer for the Solution of Tangents*

F. S. PRESTON†

Summary—**This paper describes an electrical computer employing a modified Wheatstone bridge to compute the tangent of an angle between 0° and 90°, given the angle. It can also be used to compute one angle of a right triangle given the two sides of the triangle. It thus complements the Wheatstone bridge circuit which computes the hypotenuse from the other two sides. Only linear elements are used and the accuracy of the angular approximation can be theoretically better than one part in 70,000 and in a practical application, better than one part in 2,500.**

In addition to the development of the analog circuit, this paper briefly describes some of the design considerations which were employed to permit the analog to be used successfully in field equipment employing plug-in construction and yielding accuracies of better than 0.1 per cent.

Introduction

IN DESIGNING analog computers, the engineer must have at his command various methods of solution. Frequently, it is necessary to work with tangents. Considerable effort has been expended on various approximations[1–3] with the result that several alternate possibilities exist of varied accuracy, complexity and range. Resolvers with feedback amplifiers using either unity or nearly infinite gain have been employed. Often, the designer prefers to use techniques and components similar or compatible with the over-all computer of which the tangent computation may be only a portion.

Wheatstone bridge circuits have long been used to compute ratios or to multiply. Automatic balancing facilities employing a null-detecting amplifier which controls a servo motor driving one or more arms of the bridge to continuously maintain a balance permit these bridges to be used in a wide variety of automatic analog computer applications. Bridges have been used[4] to compute one side of a right triangle, if the other two sides were known. This paper will describe a companion bridge using only linear elements which will compute the angle given the tangent (i.e., two sides) or the inverse, namely, will compute the tangent given the angle.

Development of the Circuit

To simplify the explanation, the final circuit will be developed in several steps. Since these steps are added

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[1] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Co., Inc., New York, N. Y.; 1952.

[2] W. W. Soroka, "Analog Methods in Computation and Simulation," McGraw-Hill Book Co., Inc., New York, N. Y., p. 93; 1954.

[3] P. A. Seay, "An accurate tangent computing circuit," *REAC Newsletter*, vol. 1, August, 1954.

[4] I. A. Greenwood, J. V. Holdam, and D. Macrae, "Electronic Instruments," McGraw-Hill Book Co., Inc., New York, N. Y., pp. 136–138; 1948.

refinements, some applications may not require the full circuit. It is considered easiest to explain the calculation of the angle assuming the input to be the tangent or the sine and cosine. For the time being, the circuit will show a null indicator omitting the amplifier and servo motor. It will be assumed that the bridges are continuously in balance.

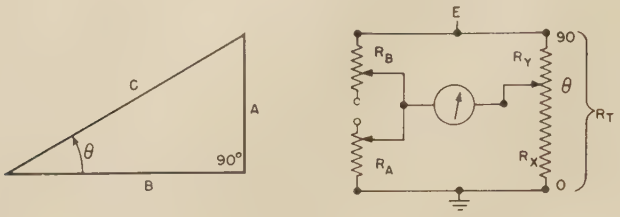


Fig. 1—Right triangle and simple approximate circuit.

In Fig. 1, the right triangle is labeled with appropriate symbols. Also shown is a circuit which approximates the solution of the angle θ' given the two sides A and B. In the text and equations to follow, θ' is the actual geometric angle and θ is the computed angle.

Let

$$R_A = K_1 A,$$
$$R_B = K_2 B,$$
$$R_X = K_3 R_T \theta,$$
$$R_Y = K_3 R_T (90 - \theta),$$

where K_1, K_2 are scale factors having units of ohms per unit length, and R_T is the nominal total resistance between the 0° and 90° points.

$$K_3 = 1/90 \text{ (nominally)}.$$

Then at balance

$$\frac{K_1 A}{K_2 B} = \frac{K_3 R_T \theta}{K_3 R_T (90 - \theta)}. \tag{1}$$

With proper selection of scale factors, K_1 and K_2 may be made equal, yielding

$$A/B = \frac{\theta}{90 - \theta}, \tag{2}$$

and from geometry

$$A/B = \tan \theta'. \tag{3}$$

However, only an approximate analog has been formed since

$$\tan \theta' \neq \frac{\theta}{90 - \theta}. \tag{4}$$

A brief examination of (4) and Fig. 1 will show, however, that the epproximation is exactly correct at three angles, namely, 0°, 45° and 90°, corresponding to tangents of 0, 1 and infinity. A plot of the error as a function of angle is shown in Fig. 2.

The simple circuit can be altered in many ways. As

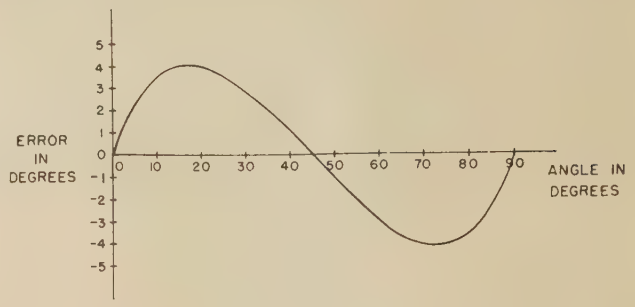


Fig. 2—Error in approximation shown in Fig. 1.

an example, assume that a resistance, R_Z, is added in shunt across R_X where

$$R_Z = K R_T \tag{5}$$

The balance equation than reduces to

$$A/B = \left(\frac{\theta}{90 - \theta}\right)\left(\frac{90K}{\theta + 90K}\right) \approx \tan \theta'.$$

The error resulting from the above approximation has been plotted in Fig. 3 for three values of K; $K=1$, $K=0.5$, and $K=2.0$. It should be noted that for $K=2$, the total spread between maximum positive and maximum negative errors is less than for Fig. 2, even though $K=2$ is not the optimum value. To center the errors would merely require a fixed angular offset.

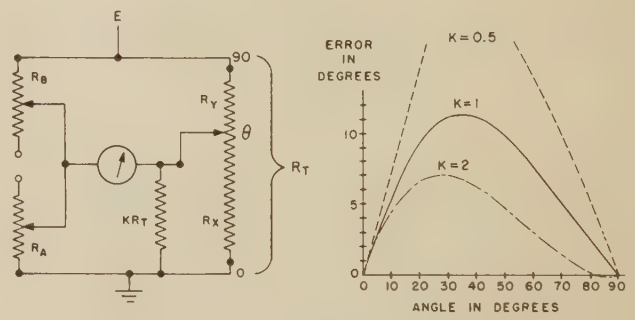


Fig. 3—Errors after adding fixed shunt across arm R_X.

Adding the fixed shunt disturbs the balance of the bridge. By changing the scale factor of either arm R_A or R_B the error curve may arbitrarily be made zero at any angle between 0° and 90° corresponding to the 45° case in (4). This change in scale factor can readily be made either by altering the resistance value or the amount of rotation to change the effective values of K_1 or K_2. To clarify the equations, it will be assumed that the values for the K's do not change, but that an additional correction, N, is applied so that $NK_1 = K_2$ where N might be considered a gear ratio. The balance equation for the circuit of Fig. 3 then becomes

$$A/B = \left(\frac{\theta}{90 - \theta}\right)\left(\frac{90KN}{\theta + 90K}\right) \approx \tan \theta'. \tag{7}$$

For the three different values of K used before, a value of N was found that resulted in zero error in the ap-

proximation at 45°. The corresponding values are given below:

For

$K = 1 \qquad N = 1.5$

$K = 0.5 \qquad N = 2.0$

$K = 2.0 \qquad N = 1.25.$

The value for N indicates that the resistance per unit of R_B should be decreased either by changing the value of R_B or by using a higher scale factor in the drive that varies R_B. The errors associated with the above set of conditions are plotted in Fig. 4. It can be shown that 45° is not the optimum value to minimize the errors nor is a shunt across arm R_X equal to R_T necessarily optimum. A selection of optimum values will yield errors less than plus or minus 0.5 degree.

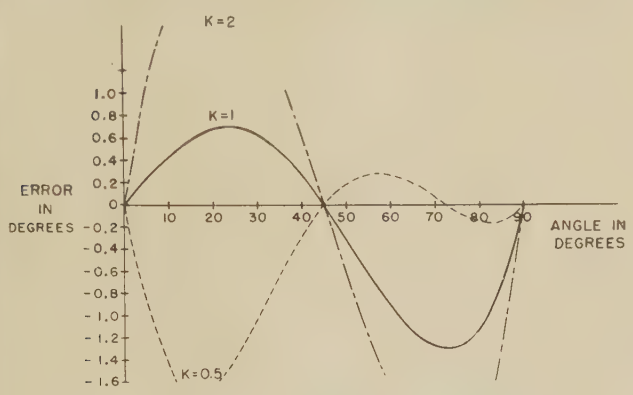


Fig. 4—Errors after adjusting scale factor of R_B.

It would now be desirable to determine the proper value for the shunt resistance which would yield zero errors. The resistance value, however, is dependent upon both the value chosen for N and that chosen for K. If one chooses to use linear elements to approximate the proper value for R_Z, it would be desirable to limit the approximation to a second order polynomial which can very easily be generated with a constant resistor in series with two linear potentiometers, one of which is short-circuited. If one solves for R_Z (with $N=1$) the following equation is obtained:

$$R_Z = \frac{\theta\left(\frac{\pi}{2} - \theta\right)\tan\theta}{\theta - \left(\frac{\pi}{2} - \theta\right)\tan\theta} R_T, \qquad (8)$$

where θ is in radians. Approximaating (8) with a second-order equation yields excessive errors. If the $\tan\theta$ function is expressed as a series expansion, it can be shown that multiplying the tangent by $2/\pi$ reduces the order of the equation permitting a better approximation. This corresponds to a value of $N=\pi/2$ which, as previously explained, can be obtained by a change in resistance for arm R_B or by a gearing change. Making this substitution yields the following:

$$R_Z = \frac{\frac{2}{\pi}\left(\frac{\pi}{2} - \theta\right)\theta\tan\theta}{\theta - \left(\frac{\pi}{2} - \theta\right)\frac{2}{\pi}\tan\theta} R_T, \qquad (9)$$

where θ is in radians. A check of the errors resulting from approximating (9) with a second-order equation indicates that an excellent approximation is possible. Thus, the optimum value for N is apparently $\pi/2$. and K for (7) would be 1.7519. The value of R_Z could be obtained assuming $R_Z = A_0 + A_1\theta + A_2\theta^2$ directly from (9). However, R_Z has no effect on the bridge at $\theta = 0$ and $\theta = 90°$. Therefore, the value of R_Z was calculated as a

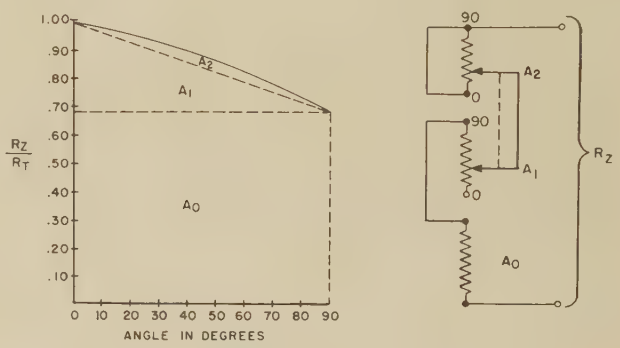
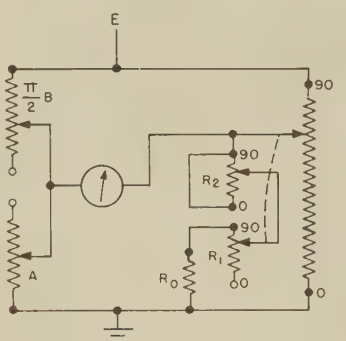


Fig. 5—Value of correcting resistance.

function of θ. This value is plotted in Fig. 5, which also shows the circuit used to obtain the approximation. The values of A_0, A_1, and A_2 were obtained by least squares curve fitting. The final circuit is shown in Fig. 6 with the values of the resistances shown as well as the gear ratio on R_B. The error in the approximation is better than one



For $\frac{\pi}{2}$

$R_0 = 0.681476 \; R_T$

$R_1 = 0.318524 \; R_T$

$R_2 = 0.141981 \; R_T$

$R_A = R_B = 1.000000 \; R_T$

For $\frac{11}{7}$

$R_0 = 0.68145 \; R_T$

$R_1 = 0.31518 \; R_T$

$R_2 = 0.14383 \; R_T$

$R_A = R_B = 1.00000 \; R_T$

Fig. 6—Final circuit and resistance values.

part in 70,000 from 0° to 90°. with corresponding accuracy when used to produce the tangent. The angular error curve is plotted in Fig. 7 on page 104.

When used to produce a tangent of a given angle, the servo motor is connected to resistance arm A (see Fig. 6). Arm B is selected as a fixed resistance of proper value for the scale factors chosen and the input angle is made to drive the three brushes of R_1, R_2, and R_T. Since the

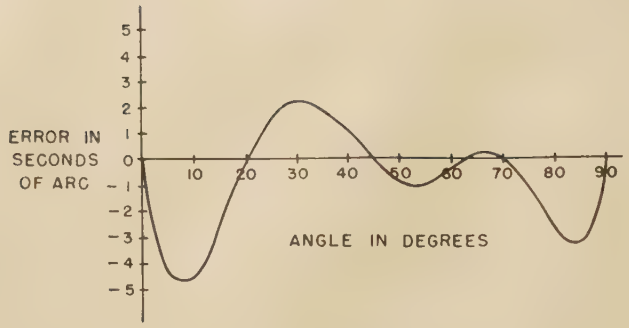


Fig. 7—Error curve for final circuit.

balance equation has been shown to give an analog to accuracies of better than ± 0.001 per cent, the following equation holds nearly exactly:

$$R_A = \frac{\pi}{2} R_B \tan \theta' = K \tan \theta'. \qquad (10)$$

Two numerical examples of the above will be given to indicate the solution. Let $R_B = (\pi/2)\ 10{,}000 = 15{,}708$ ohms. Let $R_A = 10{,}000$ ohms at $\tan \theta = 1.0000$ (therefore $K = 0.0001$). Values of R_0, R_1, and R_2 are as given in Fig. 6.

Example 1

At $\theta = 20°$ the value of the shunt R_Z is

$$R_Z = 0.681476R_T + \frac{70}{90}(0.318524R_T) + \frac{\frac{70}{90}(0.14198)\left(\frac{20}{90}\right)(0.14198)R_T^2}{0.14198R_T} = 0.9537566R_T.$$

At balance

$$\frac{R_A}{15{,}708} = \frac{\dfrac{(0.953757R_T)\left(\frac{20}{90}R_T\right)}{\left(0.953757R_T + \frac{20}{90}R_T\right)}}{\left(\frac{70}{90}\right)R_T} = 0.2317234$$

$R_A = 3{,}639.91$ $\qquad \tan \theta = 0.363991.$

Actual value $\qquad \tan 20° = 0.363970.$

Example 2

At $\theta = 60°$ the values of shunt R_Z are

$$R_Z = 0.681476R_T + \frac{30}{90}(0.318524R_T) + \left(\frac{30}{90}\right)\left(\frac{60}{90}\right)(0.14198R_T) = 0.8192018R_T$$

$$\frac{R_A}{15{,}708} = \frac{\dfrac{(0.8192018R_T)\left(\frac{60}{90}R_T\right)}{\left(0.8192018R_T + \frac{60}{90}R_T\right)}}{\frac{30}{90}R_T} = 1.102657$$

$R_A = 17{,}320.54$ $\qquad \tan \theta_2 = 1.732054$

Actual value $\qquad \tan 60° = 1.732051.$

The value of R_B may need to be changed if it is desired to operate near 90° in order to change the scale factor K in (10).

Design Details

In order to obtain a practical solution and mechanize this analog, a number of refinements were necessary. These are described separately in the following paragraphs.

Previously, it has been shown that the optimum ratio between the scale factors of arm A to arm B is $\pi/2$. Since this would impose a problem in gearing, several approximations to this were investigated. It was found that 11/7 would yield equivalent accuracies. If no change in resistance values were made, the accuracy would be no better than the approximation; i.e., one part in 2,500. By refitting the second-order equation to (9) with 7/11 replacing $2/\pi$, new values of R_0, R_1, and R_2 were found and are shown in Fig. 6.

In the foregoing, it has been assumed that perfect variable resistance elements are being used. In practice, it is relatively easy to obtain units linear to ± 0.025 per cent. This is sufficient for the single unit used on the angle, provided the resistance at each end of the travel (i.e., 0° and 90°) is quite small. Further, for ease in substitution, it is desirable that the scale factor of degrees of potentiometer rotation vs degrees of the angle be closely maintained. These criteria are not sufficient for *arms A* and *B*. Here, it is desirable that the scale factors be equal. This requires a close control on the slope of ohms per degree of rotation, or in other words, close tolerance on the total resistance as well as on the linearity. To avoid this severe problem, the gearing to one resistance element was made adjustable so that the slope of one could be varied until it matched that of the other. This is shown schematically in Fig. 8; also the mechanical arrangement to accomplish this is shown. The deviation of the slope from the nominal (or 100 per cent) value, including its algebraic sign, was stamped on the nameplate of each resistance. The ratio of the two slopes is the necessary correction which must be applied to one. A tolerance of 1 per cent was permitted. The ratio, falling between 0.98 and 1.02, could accurately be determined by subtracting one slope constant from the other. (The approximation in this simplification was taken into account in the table of desirable gear ratios.) This difference value was used to enter a table which

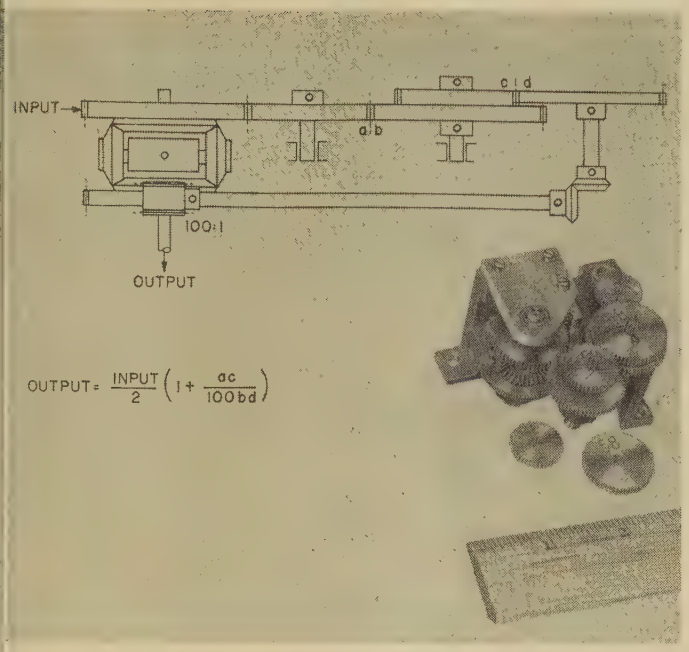


Fig. 8—Mechanism to correct for resistance slope variation.

gave the gears to use to obtain the desired ratio. Since the variable resistances were plug-in and interchangeable, it was always possible to select them so that the ratio was always positive. Therefore, it was not necessary to provide a method to subtract the correction. For convenience, fixed center distances were used in the change-gear assembly and the sum of teeth on mating gears made equal to 100. Splined shafts were used and if unity ratio was desired, no gears were added and the worm gear locked one side of the differential. A set of 23 gears permits ratios of 1.00 to 1.02 with 100 steps separated by less than ± 0.01 per cent, or ± 0.0001. As an example, assume that the ratio of two variable resistances was 1.0032. The diffreence between their two constants would be $+0.320$. The table of gear ratios would indicate the use of the following gears: 28, 72, 45, and 55 and the exact ratio would be

$$1 + \frac{(45)\cdot(28)}{(100)\cdot(55)\cdot(72)} = 1.00318.$$

All gearing, including the slope correction, was made on high speed shafts to minimize errors.

The problem of sensitivity required further circuitry. In order to protect the variable resistances from over voltage and to provide nearly a constant signal for a given amount of unbalance needed for proper servo performance, it was necessary to add a voltage control potentiometer between the power supply and the bridge. (For the tangent calculation or null detection only, a fixed series resistor suffices.) It was not possible to achieve absolutely uniform sensitivity. The actual circuit was a close approximation found empirically and consisted of a fixed resistor connecting the dc supply to a tapped resistor with brush feeding the bridge. The brush was driven by a differential such that the drive was the difference between A and B and opposite the tap when they were both zero or equal. The series resistance was therefore as given in (11):

$$\text{Series Resistance} = R_S = [0.375 + 1.125(A - B)]R_T, \quad (11)$$

where $(A-B)$ is always used as a positive value and A and B vary between 0 and 1.000.

The actual resistance values could be varied quite widely in general level but for convenience purposes $R_T = 50{,}000$ was chosen. It is readily possible to locate arms A and B in one location and the angle resistors in another and avoid the necessity of a servo system to transmit the output quantity from a computer to a sensing device. Wide temperature differences between bridge elements and locations had very little influence on the accuracy.

As previously indicated, the bridge arms were made plug-in, both mechanically and electrically (see Fig. 9). Ten-turn units were used for A, B and the main angular potentiometer. The latter was ganged to two three-turn potentiometers in the correction circuit. The plug-in feature was selected for several reasons: (1) to simplify field replacement, (2) to simplify the stock of spare parts needed since the same unit was used in several bridges, (3) to assist in the slope compensation, and (4) to eliminate the need for mechanical and electrical alignment (when replacing units) which would require high precision instruments. The final testing by the manufacturer was used to develop the slope constant which was stamped on the nameplate. This was obtained by a least squares curve fit to the measured data. This data was also used to obtain the resistance on this "best straight line" corresponding to mechanical zero. The coupling, however, was offset from mechanical zero

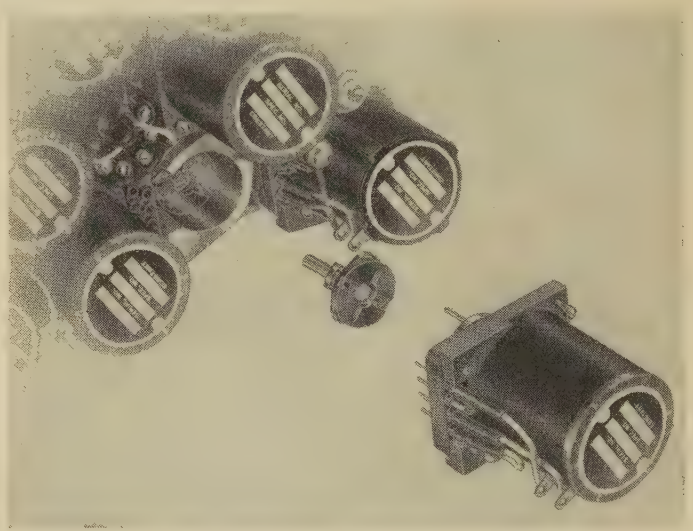


Fig. 9—View of plug-in element and mating coupling.

to compensate for this theoretical end resistance which could be either positive or negative. To accommodate this small angular offset and also to protect the resistance unit from severe mechanical shock when driven against its stops, a spring type overdrive was provided in the mating coupling which is also shown in Fig. 9.

To simplify the shielding problems, the bridge was supplied by dc rather than ac. A chopper energized by ac was used to provide an ac signal to a conventional amplifier. A reasonably good match of resistance levels between the bridge and amplifier input was possible. Although this match did not remain constant, the voltage and sensitivity control potentiometer at the bridge input compensated for any mismatch so that the over-all sensitivity varied less than ± 2 db over the entire range of useful values.

A note on final over-all accuracy should be added. The accuracy of the analog approximation to the angle is better than one part in 70,000. The accuracy of any practical application is controlled by the accuracy of the circuit elements. In one application, ± 0.025 per cent linear (or one part in 4,000) potentiometers were used. (The correction potentiometers were only ± 0.1 per cent.) The change gears could correct the slope to ± 0.01 per cent and the fixed resistor in the corrective network was matched to R_T to ± 0.02 per cent. Many units were built which met the requirement of all data better than 0.1 per cent, and 55 per cent of the data better than 0.07 per cent. Some units, in fact, were at all times better than 0.04 per cent, or one part in 2,500.

Acknowledgment

The design of this circuit was a cooperative effort and the author wishes to note the contribution of others at Norden Laboratories. Mr. Louis Wadel did much of the circuit investigation.

Closed-Loop Control Systems Containing a Digital Computer*

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Digital computers are now being considered for closed-loop control systems. This area of digital computer use is of growing importance. This review paper presents and discusses some of the consequences of introducing a digital computer into a system of this type. Computer engineers will want to be familiar with this new field of feedback systems.

The Transactions on Electronic Computers welcomes the opportunity to consider other review articles which would be of timely interest to its readers.

—*The Editor*

***Summary*—A discussion is given of the concepts of delay and distortion in feedback loops, with special reference to some of the special features incurred by digital control. Simple examples are given. Various approximations are presented for the "starred" transfer function in terms of the original analog transfer function, both in order to facilitate stability computations for digitally controlled loops, and also to illustrate the dependence of the properties of such loops on the analog and digital parameters.**

I. Introduction

THIS PAPER deals with two rather separate classes of problems concerning the behavior of simple closed-loop control systems containing a digital computer.

The first class may be regarded as treating the more "physical" aspects of such a system in that an extended discussion is given of the notions of delay and distortion in such systems, in particular, as regards the relation between the input and the fedback signal. Because of the rather different nature of such digitally controlled systems the definitions employed differ somewhat from those most common in the analysis of "continuous" systems. The "delay" of the feedback signal with respect to the input is defined both as a local property [eqs. (27) and (31)] as well as an integral property of the signal [eqs. (33), (40), (41), (43), and (44)]. The linear integral definition (33) does not have much physical significance for a digitally controlled system, though it does shed light on some aspects of the stability of the system. The quadratic integral definition, [eqs. (41), (43), and (44)] is discussed at some length with reference to a simple example. It is intimately connected with the idea of distortion (as the minimum integral of the squared deviation of the fedback and input signals), and the two are discussed together. The results are shown as curves (Figs. 10 and 11), which show how these quantities vary as the amount of feedback (K) and the total computer delay time (τ) are varied. Curves are also included showing the variation of delay and distortion in a loop with a simple analog computer having the same delay time.

The second class of problems are of a more formal nature, dealing as they do with approximate expressions for the so-called "starred" transfer functions [see (11)[7]] which enable the open-loop characteristics for the digitally controlled loop to be derived from those of the continuous loop without a computer, without re-

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course to any specific analytic form of this latter function. Approximate formulas are given for the case when the ratio of the bandwidth of the control system is small compared to that of the computer [eqs. (71), (86), and (92)], and for the cases when the computer bandwidth alone is large [see (81)]. These results are further illuminated by the discussion of the low-frequency approximation to the starred transfer function [eqs. (94), (98), and (109)]. Finally the approximation form of this starred transfer function is briefly discussed in the case of a heavily damped continuous loop.

II. Notation and Background Results

This section is devoted to stating the established results to be used, and to defining the notation. Throughout this paper the methods of frequency analysis of sampled data systems are used[1–5] together with a simplified representation of the digital computer.[6]

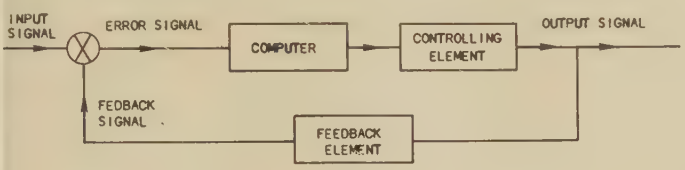

Fig. 1—Block diagram of basic system.

The basic system to be considered is shown in Fig. 1. The output of the controlling element (e.g., motor, airplane, etc.) is fedback through the feedback element, and compared with the input. The error signal (the difference between the input and the fedback signal) is then operated on by the computer, and applied to the controlling element. Introducing the complex frequency variable s by means of the Laplace transform, so that the input $i(t)$ may be represented by

$$I(s) = \int_0^\infty i(t)e^{-st}dt, \tag{1}$$

and similarly for the output $O(s)$ [$\leftrightarrow o(t)$], the feedback signal $F(s)$ [$\leftrightarrow f(t)$] and the error signal $E(s)$ [$\leftrightarrow e(t)$]. The controlling element may then be represented by a transfer function $A(s)$, and the feedback element by a transfer function $\beta(s)$. In the case of an ordinary (analog) computer, it too may be represented by a transfer function $C(s)$, and the block diagram may now be drawn as in Fig. 2.

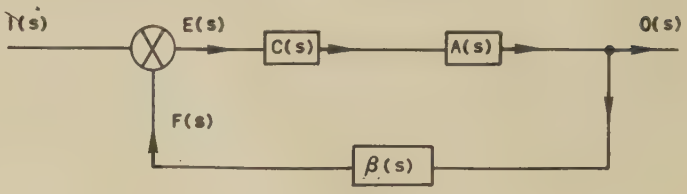

Fig. 2—Block diagram of simple analog feedback system.

One then has the following relations between the quantities of interest:

$$O(s) = \frac{C(s)A(s)}{1 + \beta(s)C(s)A(s)} I(s)$$
$$= Y_a(s)I(s), \tag{2}$$

with

$$Y_a(s) = \frac{C(s)A(s)}{1 + \beta(s)C(s)A(s)} \tag{3}$$

being the transfer function of the entire system.

$$F(s) = \beta(s)O(s) \tag{4}$$
$$E(s) = I(s)F(s). \tag{5}$$

It is convenient, for purposes of later comparison, to regard the basic system as having $C(s) \equiv 1$; i.e., no separate analog computer. This entails no loss of generality, since $C(s)$ only appears in the combination $C(s)A(s)$. Eq. (2) then becomes

$$O(s) = Y(s)I(s), \tag{6}$$

with

$$Y(s) = \frac{A(s)}{1 + \beta(s)A(s)}. \tag{7}$$

If the system includes a digital instead of an analog computer, the above relations become more complicated in quite an essential way. A digital computer may be represented most simply[6] as a sampler, a holding circuit, and a program, as shown in Fig. 3.

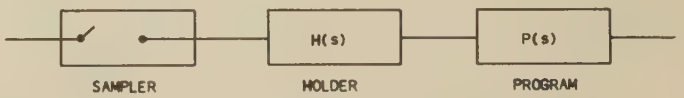

Fig. 3—Simplified model of a digital computer.

If τ is the combined sampling time, holding time, and computing time, then

$$H(s) = \frac{1}{s\tau}(1 - e^{-s\tau}); \tag{8}$$

while $P(s)$ is a quotient of two polynomials in $e^{-s\tau}$, with 1 as the leading term in the denominator. In accordance with the assumption made above regarding the analog computer, the simplest possible (and reasonable) assumption will also be made regarding the program; it will therefore be assumed that

$$P(s) = e^{-s\tau}; \tag{9}$$

[1] L. A. MacColl, "Servomechanisms," D. Van Nostrand Co., New York, N. Y.; 1945.
[2] D. F. Lawden, "A general theory of sampling servomechanisms," *Proc. IEE*, Part IV, vol. 98, pp. 31–42; January, 1951.
[3] R. H. Barker, "The pulse transfer function and its application to sampling servo systems," *Proc. IEE*, Part IV, Vol. 99, pp. 243–257; June, 1952.
[4] W. K. Linvill, "Sampled data control systems studied through comparison of sampling with amplitude modulation," *Trans. AIEE*, Part II, vol. 70, pp. 1779–1787; December, 1951.
[5] J. R. Ragazzini and L. A. Zadeh, "The analysis of sampled-data systems," *Trans. AIEE*, Part II, vol. 71, pp. 225–232; April, 1952.
[6] J. M. Salzer, "Frequency Analysis of Digital Computers Operating in Real Time," Hughes Res. and Dev. Labs. Rep.; April, 1953.

i.e., that the computer introduces a delay τ (the computing time). (It is quite easy to use computing times not equal to the sampling or holding times, but this is not significant for the present considerations.)

If an input $i(t)$ is subjected to a sampler, the output is

$$i^*(t) = \sum_{-\infty}^{\infty} \tau i(t)\delta(t - n\tau), \tag{10}$$

and its Laplace transform is[7]

$$I^*(s) = \sum_{-\infty}^{\infty} I(s + jn\Omega) \tag{11}$$

where Ω is the sampling frequency

$$\Omega = 2\pi/\tau. \tag{12}$$

If $C_d(s)$ represents the holder and the program, the block diagram of the system is as shown in Fig. 4.

The basic relations are now

$$O(s) = Y_d(s)I^*(s), \tag{13}$$

with

$$Y_d(s) = \frac{C_d(s)A(s)}{1 + [\beta(s)C_d(s)A(s)]^*}. \tag{14}$$

Eqs. (4) and (5) are unchanged.

The behavior of the entire system may be discussed in two ways. One may consider the output $o(t)$ as a function of the input $i(t)$ [or in the frequency domain $O(s)$ in terms of $I(s)$] or one may investigate only the behavior of $Y_d(s)$ in the complex s-plane, which is, of course, closely related. The first approach is most suited to the determination of properties of the system such as delay and distortion, and is the one used in the next section. The second approach is best adapted to consideration of stability, and the last two sections are devoted to results which aid in determining the behavior of $Y_d(s)$.

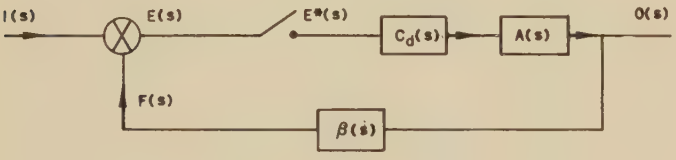

Fig. 4—Block diagram of a digital system.

It should be noted that while the loop chosen for investigation is rather simple (and will be further restricted in the following) the methods used are quite general, and may be readily extended to more complex cases, if their importance warrants it.

III. Delay and Distortion

This section is devoted to a general discussion of problems of delay and distortion[8,9] in a digitally controlled loop of the type described in the last section. this topic is rather complicated even in the analog case,[10,11] and so necessary to confine the discussion mainly to qualitative features of the general results, with illustrations by some simple specific examples.

In an ideal loop the error $e(t)$ is reduced to zero as quickly as possible, or, in other words, the fedback signal $f(t)$ approaches the input $i(t)$ as quickly as possible. It is therefore most direct to consider the behavior of $f(t)$ when investigation questions of delay or distortion in the system.

In the case of the basic loop (Fig. 2) with $C(s) \equiv 1$), one has

$$F(s) = \beta(s)Y(s)I(s), \tag{15}$$

and the fedback signal corresponding to a sinusoidal input

$$i(t) = e^{j\omega t} \tag{16}$$

is

$$f(t) = \beta(j\omega)Y(j\omega)e^{j\omega t}. \tag{17}$$

The delay is thus given by

$$\theta = \frac{1}{\omega} \arg [\beta(j\omega)Y(j\omega)]. \tag{18}$$

This definition does not however, have any simple significance for the digitally controlled loop, because the fedback signal $f_d(t)$ is no longer a simple sinusoidal function, but contains all the harmonics of the sampling frequency $\Omega = 2\pi/\tau$. Similar remarks would apply to any definition of distortion based on sinusoidal inputs: if the analog loop were slightly nonlinear, the harmonic distortion of a pure sinusoidal input would be physically significant, while even an ideal digital loop with a finite computation time would have a large amount of such distortion, with a rather different significance.

It is convenient to specialize a little in the following discussion, and to put

$$\beta(s) = \frac{K}{s} \tag{19}$$

and

$$\frac{1}{A(s)} = 1 + \alpha_1 s + \cdots + \alpha_n s^n. \tag{20}$$

[7] Eq. (11) defines the "starring" operation. In general, if $A(s)$ is the transform of any quantity of interest, then $A^*(s)$ is the transform of this quantity after it has been passed through a sampler of frequency Ω.

[8] B. H. Stafford, "Frequency Analysis of Some Closed Cycle Sample Data Control Systems," N.R.L. Rep. No. 3910: 1952.

[9] J. Sklansky and J. R. Ragazzini, "Analysis of Errors in Sampled Data Feedback Systems," Columbia University Report: 1954. This contains some related concepts.

[10] W. Jackson, ed., "Communication Theory," Thornton Butterworth, Ltd., London, England; 1953. See Chapter XXII for useful concepts of delay and distortion.

[11] R. C. Oldenbourg and H. Sartorius, "Dynamics of Automatic Control," *ASME*, New York; 1948. (Translated.) This book unfortunately came to the author's attention only after the completion of this work. It discusses in great detail problems of continuous control, from a point of view similar to that adopted here, particularly the distortion functions $\Delta(0)$ and $\delta(0)$.

These assumptions do not restrict the type of argument used, and, in fact, include many control loops of great practical importance.

From the point of view of the loops as control systems it is more illuminating to consider step function inputs as basic, in which case

$$I(s) = \frac{1}{s}, \qquad I^*(s) = \frac{\tau}{1 - e^{-s\tau}}.$$

Typical responses are illustrated in the Figs. 5 and 6.

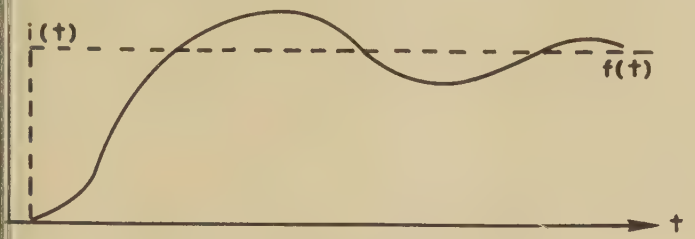

Fig. 5—Response of basic system.

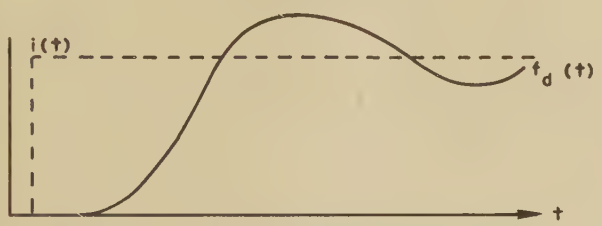

Fig. 6—Response of digitally controlled system.

The characteristic features of the responses shown above are a consequence of the assumptions (19) and (20). Since

$$\lim_{s\to\infty} F(s) = \lim_{s\to\infty} sF(s) = 0, \tag{21}$$

one has

$$f(0) = 0, \tag{22}$$

and similarly

$$f_d(t) \equiv 0, \quad \text{for} \quad t \leqq \tau. \tag{23}$$

Also, since

$$\lim_{s\to 0} sF(s) = 1, \tag{24}$$

it follows that

$$\lim_{t\to\infty} f(t) = 1 \tag{25}$$

and similarly

$$\lim_{t\to\infty} f_d(t) = 1. \tag{26}$$

(In the above formulas, and in what follows, the subscript d denotes quantities in the digital system.)

One simple definition of delay may be obtained by extrapolating the initial form of $f(t)$ [or $f_d(t)$] and determining the value of $t=\theta$ for which this extrapolation is unity. (See Fig. 7).

Noting the forms (19) and (20) assumed for $\beta(s)$ and $A(s)$, and the fact that $s^mF(s)$ is the Laplace transform of $f^{(m)}(t)$, it is easy to compute the form of $f(t)$ for small t. This turns out to be

$$f(t) \simeq \frac{1}{(n+1)!}\left(\frac{K}{\alpha_n}\right) t^{n+1}, \tag{27}$$

whence

$$\theta = \left[(n+1)!\,\frac{\alpha_n}{K}\right]^{1/n+1}. \tag{28}$$

For example, if $A(s) = 1$,

$$\theta = \frac{1}{K}; \tag{29}$$

and if

$$A(s) = \frac{1}{1+T_s},$$

$$\theta = \sqrt{\frac{2T}{K}}. \tag{30}$$

A similar computation for $f_d(t)$ yields the result

$$f_d(t) \simeq \frac{1}{(n+1)!}\left(\frac{K}{\alpha_n}\right)(t-\tau)^{n+1} \tag{31}$$

for small positive $t-\tau$, so that

$$\theta_d = \tau + \theta, \tag{32}$$

θ being given by (28).

It should be noted that (28) will not have much physical significance if $\alpha_n \ll \alpha_{n-1}$, for then the form of $f(t)$ will be determined by α_{n-1} except for extremely small values of t. In such cases a more specific (and correspondingly less general and perspicuous) computation is called for.

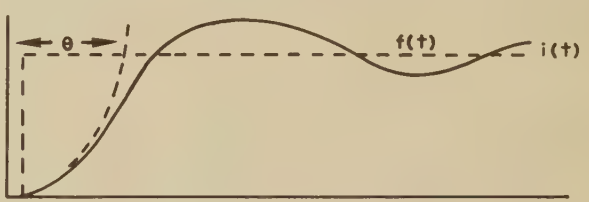

Fig. 7—Time delay in terms of the extrapolated initial form.

The above results indicate that the digital system has an additional delay τ as compared to the basic system, but do not show any further dependence on the parameters of the loop. One would expect (intuitively) that the difference between the digital and basic loops should depend on the parameters of the actual loop. The fact that such a dependence is not shown may be attributed largely to the purely local character of this definition, depending, as it does, only on the form of the response $f(t)$ for small values of t. It does not take account of the rate or the manner in which $f(t)$ approaches its limiting value 1 (once it becomes appreciable); consequently both the low-frequency response of the system and pos-

sible instability effects are almost completely ignored by this definition. In order to remedy this defect a definition of delay involving integral (or global) properties of $f(t)$ must be considered.

The simplest definition of this type which comes to mind, and which has physical significance if $f(t)$ has no overshoot, is

$$\theta = \int_0^\infty [1 - f(t)]dt. \tag{33}$$

The physical significance of this is shown in Fig. 8. θ is the amount the input step function would have to be displaced to give the same integrated error as the actual output.

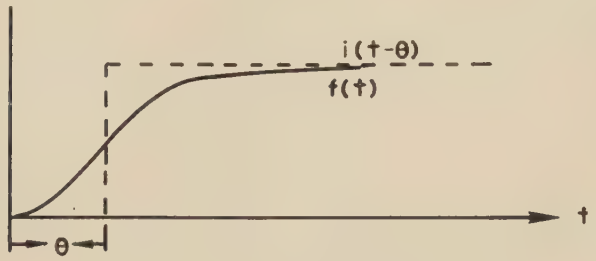

Fig. 8—Linear integral definition of delay.

With this definition θ may be evaluated simply and directly in terms of $\Gamma(s) = \beta(s)\, Y(s)$. One has

$$\begin{aligned}\theta &= \lim_{s\to 0} \int_0^\infty e^{-st}[-1 - f(t)]dt \\ &= \lim_{s\to 0}\left[\frac{1}{s} - F(s)\right] \\ &= \lim_{s\to 0} \frac{1 - \Gamma(s)}{s};\end{aligned}$$

i.e.,

$$\theta = -\Gamma'(o). \tag{34}$$

If $\beta(s)$, $A(s)$ have the forms assumed earlier, one finds easily that

$$\theta = \frac{1}{K}; \tag{35}$$

so that, disconcertingly enough, θ does not depend on the form of $A(s)$, as long as $A(0)$ is finite and $\lim_{s\to 0} s\beta(s) = K$ is finite. This definition therefore errs in the opposite way, by considering only the low-frequency behavior of the system. One may compute θ_d by using the form of the starred transfer function given in the next section,[2] it turns out that

$$\theta_d = \frac{1}{K} - \frac{1}{2}\tau = \theta - \frac{1}{2}\tau. \tag{36}$$

This result is quite surprising (and even misleading) if considered as an actual "delay," for it is clear from the previous results that for a "fast" basic system (i.e., one with small θ and large K) one should have

$$\theta_d \simeq \theta + \tau, \tag{37}$$

as far as any intuitive definition of delay goes. One does, however, obtain some interesting general information about the system if one considers these results in terms of the basic formula (33). Firstly, since $\theta_d < \theta$, the digital system always has less damping than the basic system. Since $f_d(t) = 0$ for $t \leqq \tau$, the digital system always has a delay of at least τ to start with. Taking this into account, and assuming that the digital system has no overshoot, the equivalent digital damping is less than the equivalent basic damping by the factor

$$1 - \frac{3}{2}K\tau. \tag{38}$$

It is clear therefore, that any digital system with

$$G = K\tau \geqq 2/3 \tag{39}$$

will have overshoot, though in general this will occur for even smaller values of G. In particular cases better estimates may be obtained for this limiting value for overshoot by expanding $f_d(t)$ for small values of t.

The above discussion shows some of the relations between analog and digital responses, but also indicates the need for a definition of delay which takes account both of the initial (high frequency) behavior of the response, as well as the integral (low-frequency) character. This may be best accomplished by defining the delay in terms of some positive functional of $[1 - f(t)]$, in which the larger values are weighted more heavily than the smaller ones. Any such definition, however, also involves the deviation of $f(t)$ from $i(t)$ at large values of t in a manner which does not seem particularly germane to any intuitive notion of delay. It is therefore desirable to separate in some way the "delay" and the "distortion" in such a definition. In particular, if $f(t) = i(t - \theta)$ the delay should come out to be θ and the distortion zero, while if $f(t) = i(t) + a(t)$ with $a(0) = 0$, the delay should come out to be zero, and the distortion should be the relevant positive functional of $a(t)$. A general pair of definitions is then the following.

Let $\sigma[h(t)]$ be a positive functional of $h(t)$, such that $\sigma[0] = 0$, $\sigma[h(t)] > 0$ for $h \not\equiv 0$.

Let

$$\Delta(\theta) = \sigma[i(t - \theta) - f(t)]. \tag{40}$$

The *delay* θ is then defined as that value of θ for which $\Delta(\theta)$ is a minimum; i.e., for which

$$\frac{d\Delta(\theta)}{d\theta} = 0. \tag{41}$$

The corresponding value of $\Delta(\theta) = \Delta$ is then defined as the distortion. If σ is continuous and monotonic it is easy to see that Δ is now defined by

$$f(\theta) = \tfrac{1}{2}. \tag{42}$$

Δ, however, can only be computed when a specific form is taken for σ. The simplest definition, and one which is most useful in assigning physical significance to the distortion is[12]

$$\Delta^2(\theta) = \int_0^\infty [i(t-\theta) - f(t)]^2 dt. \tag{43}$$

This definition will be used in the remainder of this discussion. It should be noted that the above definitions do not depend on the use of a step input. Any time variation may be used as a standard input, and the basic method remains the same, though in general θ will not longer be defined by as simple a relation as (42).

While the general character of these formulas is quite clear, it is rather difficult to compute θ and Δ explicitly in general. The remainder of this section is therefore devoted to a comparison, in the light of the above definitions, of a very simple basic and digital loop. Before proceeding to this, however, it is worthwhile remarking, that in any complex case, $\Delta(\theta)$ is best computed in terms of the Laplace transforms of the quantities involved; viz.,

$$\Delta^2(\theta) = \frac{1}{2\pi}\int_C \left|\frac{e^{-s\theta} - \beta(s)Y(s)}{s}\right|^2 ds. \tag{44}$$

The following considerations concern the basic loop of Fig. 2 with $C(s)=A(s)=1$, $\beta(s)=K/s$, and the corresponding digital loop. For the basic loop,

$$F(s) = \frac{K/s}{1+K/s}\cdot\frac{1}{s} = \frac{1}{s} - \frac{1}{s+K}; \tag{45}$$

so that

$$f(t) = 1 - e^{-Kt}. \tag{46}$$

Thus,

$$\theta = \frac{1}{K}\log_e 2; \tag{47}$$

or, introducing $G=K\tau$,

$$\frac{\theta}{\tau} = \frac{.69}{G}. \tag{48}$$

Further,

$$\frac{\Delta^2}{\tau} = \left[\log_e 2 - \frac{1}{2}\right]/G = \frac{.193}{G}. \tag{49}$$

[12] An analogous definition is sometimes used to define distortion in communication systems: see ref.[10]. $\Delta^2(0)$ is closely related to the mean error as defined in ref.[9].

In the digital case one finds

$$F_d(s) = \frac{Ge^{-s\tau}}{1 - e^{-s\tau} + Ge^{-2s\tau}}Q(s) \tag{50}$$

with

$$Q(s) = \frac{1}{s}\cdot\frac{1-e^{-s\tau}}{s\tau}. \tag{51}$$

$F_d(s)$ may be rewritten in the form

$$F_d(s) = \frac{G}{z_1 - z_2}\sum_0^\infty (z_1^n - z_2^n)e^{-ns\tau}Q(s), \tag{52}$$

where

$$z_{1,2} \pm \tfrac{1}{2} - \tfrac{1}{2}\sqrt{1-4G}. \tag{53}$$

Hence,

$$f_d(t) = \frac{G}{z_1 - z_2}\sum_0^\infty (z_1^n - z_2^n)q(t-n\tau); \tag{54}$$

with

$$q(t) = \begin{cases} 0 & t \leqq 0 \\ \dfrac{t}{\tau} & 0 \leqq t \leqq \tau \\ 1 & t > \tau. \end{cases} \tag{55}$$

One may now compute θ_d and Δ_d for different values of G. The explicit formulas are not given here, for $f_d(t)$ has a different form in each interval, and consequently θ_d and Δ_d have different analytic forms for different values of G.

The results of these computations are plotted in Figs. 9 and 10 on page 112. In order to enable simpler interpretation to be made of the effect of the digital computer (in terms of an analog element) curves are also included of θ_a and Δ_a, the delay and distortion for a simple analog loop with

$$C(s)A(s) = \frac{1}{1+\tau s}. \tag{56}$$

(The explicit formulas are not given here, for they are rather messy and not very informative.) Fig. 10 also contains curves of the quantity

$$\delta^2 = \int_0^\infty 0^2(t)dt = \frac{1}{2\pi}\int_C \left|\frac{Y(s)}{s}\right|^2 ds, \tag{57}$$

which gives a measure of the output fluctuation required to control the system. For the simple loops considered above one readily computes that

$$\frac{\delta^2}{\tau} = \frac{1}{2G} \tag{58}$$

$$\frac{\delta_a^2}{\tau} = \frac{1}{2G}, \tag{59}$$

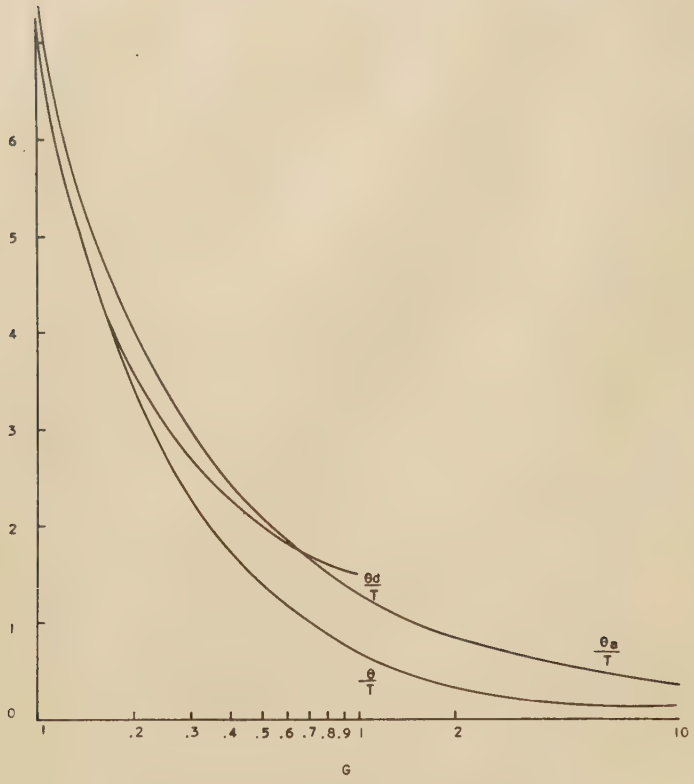

Fig. 9—Delay curves for simple loops.

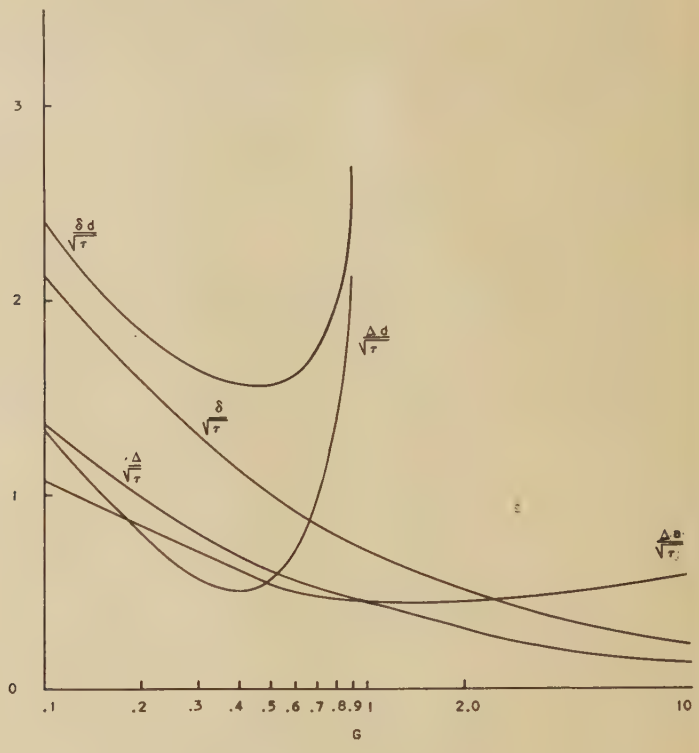

Fig. 10—Distortion and output fluctuation curves.

and

$$\frac{\delta_a^2}{\tau} = \frac{1}{2G}\,\frac{1+G}{(1-G)\left(1+\frac{1}{2}G\right)}. \qquad (60)$$

Among the general features illustrated by the curves are the following:

1. The digital loop is limited to the region $G \leqq 1$ for stability reasons. Since instability occurs as $G \to 1$, the distortion $\Delta_d \to \infty$ in this limit, as well as for $G \to 0$. The delay $e^{-s\tau}$ leads to comparatively large values of θ_d for $G \to 1$, but with decreasing G, θ_d becomes less than θ_a, and approaches θ, because of the smoothing effect of the holding element $(1-e^{-s\tau})/s\tau$ which becomes important in this region. For the same reason Δ_d becomes less than Δ_a or Δ in this region. On the other hand δ_d is always greater than δ_a or δ.
2. For a fixed computing time τ, the equivalent analog and digital systems have respectively minimum distortions of $.45\sqrt{\tau}$ and $.49\sqrt{\tau}$, with corresponding delays of 1.29τ and 2.25τ, and corresponding gains (K) of $1/\tau$ and $.4/\tau$. Thus if τ can be arbitrarily reduced, the delays and distortions can be made as small as desired, but otherwise, the introduction of a computer definitely degrades the performance of the loop. However, if there are gain limitations on the loop, the digitally controlled loop may give an appreciable advantage distortion-wise at the cost of only a slight additional delay.

It should be noted, in general, for a more complicated basic element $A(s)$, there will be stability restrictions on G in the case of the basic and equivalent analog loops too. The curves of θ, θ_a, and Δ, Δ_a will then resemble those of θ_d and Δ_d more closely though the limiting G value will generally be larger. It is also noteworthy, as indicated above, that while the delay is a monotonically decreasing function of K, this is not usually so for the distortion or the output fluctuation, and it is therefore necessary to design the system with an eye not only to delay limitations, but also to those imposed by distortion effects.

Finally, it may be remarked again that the above considerations may be readily extended to computers with programs, to control loops with arbitrary $A(s)$ and $\beta(s)$, and to more complex loops, at the cost of rather more computation.

IV. Approximate Forms of "Computed" Transfer Functions

Referring back to the remarks of Section II, and, in particular, to (7)

$$Y(s) = \frac{A(s)}{1+\beta(s)A(s)}$$

and (14)

$$Y_d(s) = \frac{C_d(s)A(s)}{1+\beta[C_d(s)\beta(s)A(s)]^*},$$

it is clear that the essential relations between $Y(s)$ and $Y_d(s)$ may be readily obtained, once the relation between

$$\Gamma(s) = \beta(s)A(s) \qquad (61)$$

and

$$\Gamma_d(s) = [C_d(s)\beta(s)A(s)]^* \tag{62}$$

is known.

If $\beta(s)=1/s$ and $A(s)$ is given as partial fraction expansion in s, then the expression for $\Gamma_d(s)$ can, of course, be computed (formally) quite directly, using the results of reference 1. In fact, if

$$A(s) = \sum_1^n \frac{a_k}{s - s_k}, \tag{63}$$

so that

$$\Gamma(s) = \frac{A(s)}{s} = \sum_0^n \frac{a_k}{s_k(s - s_k)}, \quad \text{with}$$

$$s_0 = O\frac{a_0}{s_0} = A(O) \text{ (defn.)} \tag{64}$$

then

$$\Gamma_d(s) = \frac{e^{-(3/2)s\tau}}{\cosh \frac{1}{2}\tau s} \sum_0^n \frac{(a_k/s_k)}{\left(\frac{\tau s_k}{2}\coth\frac{s_k}{2}\right)\left(\frac{2}{\tau}\tanh\frac{\tau s}{2}\right) - s_k}, \tag{65}$$

and this expression may, of course, be transformed in many different ways.

Unfortunately, this last expression is not terribly perspicuous, nor is $A(s)$ generally given in the partial fraction form cited above, but rather as a function of $s=j\omega$ in graphical form (Nyquist or log-mod and phase diagrams). One would therefore like some more direct relation between $\Gamma_d(s)$ and $A(s)$ in terms of more intrinsic properties of the latter, and not involving recourse to the particular form in which $A(s)$ is expressed.

Before proceeding to any computation one may note that since

$$C_d(s) = e^{-s\tau}(1 - e^{-s\tau})/s\tau, \tag{66}$$

by virtue of the assumptions in Section II, one has

$$\Gamma_d(s) = e^{-(3/2)s\tau}\left(\frac{2}{\tau}\sinh\frac{s\tau}{2}\right)\left[\frac{A(s)}{s^2}\right]^*; \tag{67}$$

so that only $[A(s)/s^2]^*$ need enter into the calculations. Further, since any starred transfer function $T^*(s)$, say, satisfies the relations

$$T^*(s + jn\Omega) = T^*(s) \tag{68}$$

and

$$T^*(j\omega + \tfrac{1}{2}j\Omega) = \overline{T}^*(-j\omega + \tfrac{1}{2}\Omega) \tag{69}$$

(where Ω is the sampling frequency $2\pi/\tau$, and the bar denotes complex conjugation), it is only necessary to consider complex frequencies $s=j\omega$ for which $\omega \leqq \frac{1}{2}\Omega$.

From the basic definition

$$\left[\frac{A(s)}{s^2}\right]^* = \sum_\infty^\infty \frac{A(s + jn\Omega)}{(s + jn\Omega)^2} = \frac{A(s)}{s^2} + \frac{A(s + j\Omega)}{(s + j\Omega)^2} + \frac{A(s - j\Omega)}{(s - j\Omega)^2} + \cdots, \tag{70}$$

it is clear that if the bandwidth s_c of A is small compared to the sampling frequency Ω (i.e., if $s_c\tau \ll 1$) then the first term in the sum above should give a good approximation to the starred quantity of the left. In that case, one has, approximately,

$$\Gamma_d(s) \simeq e^{-(3/2)s\tau}\left(\frac{2}{\tau}\sinh\frac{s\tau}{2}\right)\frac{A(s)}{s^2}; \tag{71}$$

or, placing $s=j\omega$,

$$\Gamma_d(j\omega) \simeq e^{-(3/2)j\omega\tau}\left(\frac{\sin\frac{1}{2}\omega\tau}{\frac{1}{2}\omega\tau}\right)\left(\frac{A(j\omega)}{j\omega}\right). \tag{72}$$

In this case, therefore, the effect of the computer is to introduce a delay $(3/2)\tau$ and a smoothing function $(\sin\frac{1}{2}\omega\tau/\frac{1}{2}\omega\tau)$ into the open loop transfer function $A(s)/s$.

The above result may be made more precise in several ways. The condition that the bandwidth of $A(s)$ be small compared to the sampling frequency Ω, may be restated as

$$|s_k\tau| \ll 1 \qquad k = 1, \cdots n, \tag{73}$$

where the s_k are the (complex) poles of $A(s)$. This condition may be satisfied if either τ or the s_k are sufficiently small.

Suppose to begin with that τ is small. Now,

$$\frac{A(s)}{s^2} = \frac{A(0)}{s^2} + \frac{A'(0)}{s} + \sum_1^n \frac{a_k}{s_k^2(s - s_k)}, \tag{74}$$

with

$$A(0) = -\sum \frac{a_k}{s_k} \quad \text{and} \quad A'(0) = -\sum \frac{a_k}{s_k^2}. \tag{75}$$

Then

$$\left(\frac{A(s)}{s^2}\right)^* = A(0)\left(\frac{\tau^2}{4}\operatorname{cosech}^2\frac{s\tau}{2}\right) + A'(0)\frac{\tau}{2}\left(\coth\frac{s\tau}{2} + 1\right) + \sum_1^n \frac{a_k}{s_k^2}\frac{\tau}{2}\left(\coth\frac{(s - s_k)\tau}{2} + 1\right). \tag{76}$$

Expanding the various terms as power series in τ, and recombining the various coefficients, one finds that

$$\left(\frac{A(s)}{s^2}\right)^* = \frac{A(s)}{s^2} + \frac{\tau^4}{240}\left[\tfrac{1}{3}\sum a_k s_k - s\sum a_k\right] + \frac{\tau^4}{6048}\left[-\sum a_k s_k^3 + s\sum a_k s_k^2 - 2s^2\sum a_k s_k + 2s^3\sum a_k\right] + \cdots.$$

Introducing the impulse response of $A(s)$.

$$a(t) = \frac{1}{2\pi j}\int_C A(s)e^{st}ds, \tag{77}$$

one easily finds that

$$\sum a_k s_k{}^m = a^{(m)}(0), = a_o{}^{(m)}, \tag{78}$$

or, in terms of $A(s)$,

$$a_o = \lim_{s\to\infty} sA(s)$$
$$a_o{}^{(1)} = \lim_{s\to\infty} s[A(s) - a(o)], \tag{79}$$

etc. Thus

$$\left(\frac{A(s)}{s^2}\right)^* = \frac{A(s)}{s^2} + \frac{\tau^4}{240}\left[\frac{1}{3}a_o{}^{(1)} - sa_o\right] + \frac{\tau^6}{6048}\left[-a_o{}^{(3)} + sa_o{}^{(2)} - 2s^2a_o{}^{(1)} + 2s^3a_o\right] + \cdots, \tag{80}$$

or

$$\Gamma_d(s) = e^{-(3/2)s\tau}\left\{\frac{\sinh\frac{s\tau}{2}}{s\tau/2}\right\} \cdot \left\{\frac{A(s)}{s} + \frac{\tau^4}{240}\left[\frac{1}{3}sa_o{}^{(4)} - s^2a_o\right] + \cdots\right\}. \tag{81}$$

i.e., the digital "open loop" transfer function is obtained from the analog open loop transfer function $A(s)/s$, by adding to the latter a series of correction terms in powers of τ, viz.,

$$\frac{\tau^4}{240}\left[\frac{1}{3}sa_o{}^{(1)} - s^2a_o\right] + \frac{\tau^6}{6048}[\cdots]\cdots, \tag{82}$$

and multiplying the entire sum by a delay $e^{-3/2s\tau}$ and a smoothing factor $(\sinh s\tau/2/s\tau/2)$. It is clear since $a_o{}^{(m)}\sim s_c{}^m$ and $A(j\Omega/2)$ is small, that the above approximation will break down unless $s_c\tau$ is small.

One may arrive at a result in a rather different form, by considering the quantity s_k as sufficiently small. Referring to (65), one may expand $\left[\frac{\tau s_k}{2}\right]\coth \tau s_k/2$ as a power series in s_k,

$$\frac{\tau s_k}{2}\coth\frac{\tau s_k}{2} = 1 + \frac{\tau^2}{12}s_k{}^2 - \frac{\tau^4}{720}s_k{}^4 + \cdots \qquad (|\tau s_k| < 2\pi). \tag{83}$$

Then

$$\Gamma_d(s) = \frac{e^{-(3/2)s\tau}}{\cosh\frac{s\tau}{2}} \cdot \sum_0^n \frac{(a_k/s_k)}{\left(1 + \frac{\tau^2}{12}s_k{}^2 + \cdots\right)\left(\frac{2}{\tau}\tanh\frac{s\tau}{2}\right) - s_k}. \tag{84}$$

Taking some typical figures

$$\tau = \frac{1}{6}, \qquad |s_k| = \frac{3}{\sqrt{2}},$$

(83) has terms of the order

$$1, \quad \frac{1}{96}, \quad \frac{1}{45000}, \cdots.$$

In most cases therefore it will be adequate to consider only the first or first two terms of the series. With such approximations $\Gamma_d(s)$ assumes comparatively simple expressions in terms of $\Gamma(s) = A(s)/s$.

Suppose firstly that it is permissible to put

$$\frac{\tau s_k}{2}\coth\frac{\tau s_k}{2} \simeq 1. \tag{85}$$

Then[13]

$$\Gamma_d(s) \simeq \frac{e^{-(3/2)s\tau}}{\cosh\frac{1}{2}s}\sum_0^n \frac{(a_k/s_k)}{\frac{2}{\tau}\tanh\frac{s\tau}{2} - s_k} = \frac{e^{-(3/2)s\tau}}{\cosh\frac{1}{2}s\tau}\,\Gamma\left(\frac{2}{\tau}\tanh\frac{\tau s}{2}\right). \tag{86}$$

Note that this approximation will break down for $s\cong s_k$. Since, however, one is only interested in $\Gamma_d(s)$ and $\Gamma(s)$ for $s = j\omega$, and since $\mathrm{Re}(s_k) < 0$, this fact will not generally cause much trouble. The error terms contain $(s - s_k)$ in the denominator, hence the approximation will be better the larger $|\mathrm{Re}(s_k)|$. Taking $s = j\omega$, (86) becomes

$$\Gamma_d(j\omega) = \frac{e^{-(3/2)j\omega t}}{\cos\frac{\omega\tau}{2}}\,\Gamma\left(\frac{2j}{\tau}\tan\frac{\omega\tau}{2}\right). \tag{87}$$

Now suppose that a more accurate representation is required, and that the approximation

$$\frac{\tau s_k}{2}\coth\frac{\tau s_k}{2} \simeq 1 + \frac{\tau^2}{12}s_k{}^2 \tag{88}$$

is adequate. Then

$$\Gamma_d(s) = \frac{e^{-(3/2)\tau s}}{\cosh\frac{s\tau}{2}} \cdot \sum_0^n \frac{(a_k/s_k)}{\left(1 + \frac{\tau^2}{12}s_k{}^2\right)\left(\frac{2}{\tau}\tanh\frac{s\tau}{2}\right) - s_k}. \tag{89}$$

The denominators of the partial fractions are quadratics in s_k, and each term may therefore be decomposed into a sum of two partial fractions, the denominator of each being linear in s_k; i.e.,

[13] This type of approximation was first given by H. Raymond, *Ann. Telecommun.*, vol. 4, pp. 250, 307, 347; 1949.

$$\frac{1}{(1+cs_k^2)u-s_k}=\frac{1}{\sqrt{1-4cu^2}}\cdot\left\{\frac{2cu}{1-\sqrt{1-4cu^2}-2cus_k}-\frac{2cu}{1+\sqrt{1-4cu^2}+2cus_k}\right\},$$

where

$$c=\frac{\tau^2}{12},\qquad u=\frac{2}{\tau}\tanh\frac{s\tau}{2}.$$

Placing

$$p(s)=\frac{1-\sqrt{1-4cu^2}}{2cu}$$

$$=\frac{3}{\tau}\left[\coth\frac{s\tau}{2}-\sqrt{\operatorname{cosech}^2\frac{s\tau}{2}-\frac{1}{3}}\right],\qquad(90)$$

one finds that

$$\Gamma_d(s)-\frac{e^{-(3/2)s\tau}}{\sqrt{1-\frac{1}{3}\sinh^2\frac{s\tau}{2}}}\left\{\Gamma[p(s)]-\Gamma\left(\frac{12}{\tau^2p(s)}\right)\right\}\qquad(91)$$

(where $\Gamma[p(s)]=1/p(s)A[p(s)]$, etc.).

Similar remarks to those following (86) also apply in this case regarding the degree of approximation and the size of $|\mathrm{Re}(s_k)|$. Placing $s=j\omega$.

$$\Gamma_d(j\omega)-\frac{e^{-(3/2)j\omega t}}{\sqrt{1+\frac{1}{3}\sin^2\frac{\omega\tau}{2}}}\left\{\Gamma[p(j\omega)]-\Gamma\left(\frac{12}{\tau^2p(j\omega)}\right)\right\},\qquad(92)$$

with

$$p(j\omega)=\frac{3j}{\tau}\left[\sqrt{\operatorname{cosec}^2\frac{\omega\tau}{2}+\frac{1}{3}}-\cot\frac{\omega\tau}{2}\right].\qquad(93)$$

The following comments may be made regarding the above approximations. Eqs. (87) and (93) both have the advantage of satisfying the basic periodicity properties (68) and (69) of starred transfer functions. The approximation given by (81) does not have this property unless the entire infinite sum is included. They have the further convenient feature that apart from a multiplicative factor (which occurs in all approximations) and a rather simple change of scale

$$\left[\text{i.e., } s\to\frac{2}{\tau}\tanh\frac{s\tau}{2}\text{ or }s\to p(s)\simeq s\left(1-\frac{\pi^4}{1260}\frac{s^4}{\Omega^4}\right)\right]$$

they are expressed directly in terms of $\Gamma(s)=A(s)/s$, without additional additive terms such as appear in (81). On the other hand, they have the disadvantage that by their very nature

$$\Gamma_d\left(j\frac{\Omega}{2}\right)=0.$$

While it is true that because of the narrow bandwidth this should not significantly affect many computations, it may nevertheless lead to appreciable error in computations involving the high-frequency behavior (e.g., if the input noise power is peaked at a frequency near $\Omega/2$).

Having carried out expansions with respect to τ and the s_k one is naturally led to inquire what the effect is of an expansion with respect to the frequency variable s itself. As will appear below, the main interest of this method lies in the extent to which it illuminates the degree of approximation obtained by finite sum approximations of starred transfer functions; i.e., it enables one to estimate the size of the "error" term $R_m(s)$ in the expression

$$\left(\frac{A(s)}{s^2}\right)^*=\sum_{-\infty}^{+\infty}\frac{A(s+jn\Omega)}{(s+jn\Omega)^2}=\sum_{-m}^{m}\frac{A(s+jn\Omega)}{(s+jn\Omega)^2}+R_m(s).\qquad(94)$$

It might be remarked that such a separation (with $m=0$) is required even when one is interested in the Taylor series alone, simply because the first term $A(s)/s^2$ is singular for $s=0$. Since

$$\frac{A(s)}{s^2}=\frac{A(0)}{s^2}+\frac{A(0)}{s}+\sum_1^n\frac{a_k}{s_k^2(s-s_k)},\qquad[\text{see (74)}]$$

one must consider the remainder terms for

$$\left(\frac{1}{s^2}\right)^*\quad\left(\frac{1}{s}\right)^*\quad\text{and}\quad\left(\frac{1}{s-s_k}\right)^*$$

and then combine them suitably.

Consider firstly[14]

$$\sum_{-\infty}^{+\infty}\frac{1}{s+jn\Omega}=\frac{\pi}{\Omega}\coth\frac{\pi_s}{\Omega}\qquad(95)$$

One may write

$$\sum_{-\infty}^{+\infty}\frac{1}{s+jn\Omega}=\sum_{-m}^{+m}\frac{1}{s+jn\Omega}+R_m{}^{(o)}(s),\qquad(96)$$

with

$$R_{m(s)}{}^{(o)}=\sum_{m+1}^{\infty}\frac{2s}{s^2+n^2\Omega^2}.\qquad(97)$$

Expanding each term as a power series in s yields the result

$$R_m{}^{(o)}(s)=-\frac{1}{s}\sum_{l=\omega}^{\infty}2c(l+1,m)\left(\frac{s}{j\Omega}\right)^{2(l+1)}\qquad(98)$$

[14] Note that actually

$$\left(\frac{1}{s}\right)^*=\frac{\pi}{\Omega}\left(\coth\frac{\pi_s}{\Omega}+1\right).$$

However, the constant terms cancel in the sum

$$\left(\frac{A'(0)}{s}\right)^*+\sum^n\frac{a_k}{s_k^2}\left(\frac{1}{s-s_k}\right)^*.$$

with

$$c(l+1, m) = \sum_{n=m+1}^{\infty} \frac{1}{n^{2(l+1)}}. \tag{99}$$

The reason for writing the result in this form is that it enables easy comparison with the leading term in the original expression $(1/s)$, and the result is rendered more perspicuous when $s=j\omega$ because $s/j\Omega$ then becomes equal to $x=\omega/\Omega$ which need only be considered in the range $0<x<.5$. [See the remarks following (69)]. The following table indicates the behavior of $c(l+1, m)$.

m/l	0	1	2
0	1.6449	1.0823	1.0173
1	.6449	.0823	.0173
2	.3949	.0198	.0017
3	.2838		

(100)

For large enough l, and $m>0$,

$$c(l+1, m) \simeq (m+1)^{-2(l+1)}. \tag{101}$$

As a consequence of these properties and the fact that $x<\frac{1}{2}$, it follows that the first term in $R_m^{(o)}(s)$ will give the major contribution to the sum, and may therefore generally be used as a good approximation to it. As an example, the difference between $\pi\cot\pi x$ and

$$\frac{1}{x} - \frac{2x}{1-x^2} - 1.290x$$

[corresponding to the approximation with $m=1$, and only including the first term in $R_1^{(o)}(s)$] varies between 0(for $x=0$) and .0216 (for $x=.5$). This approximation remains quite good up to $x\cong 1$, since the singularity at that point is taken care of. On the other hand, taking $m=0$ (i.e., including only the leading term in the original sum) and using two terms in the series for $R_o^{(o)}(s)$ leads to an approximation which is very good for $x\leqq .5$, but rather poor for $x>.5$. The approximation

$$\frac{1}{x} - \frac{2x}{1+x^2}$$

(i.e., including the three leading terms in the original sum, but none of the remainder) leads to an error of .66 for $x=.5$, which makes it quite inadequate.

The above discussion becomes more significant when one proceeds to the consideration of

$$\sum_{-\infty}^{+\infty} \frac{1}{s-s_k+jn\Omega} = \sum_{-m}^{+m} \frac{1}{s-s_k+jn\Omega} + R_m^{(k)}(s). \tag{102}$$

$R_m^{(k)}(s)$ has the same form as $R_m^{(o)}(s)$, with s replaced by $s-s_k$. However, the condition $|s/\Omega|<\frac{1}{2}$ does not necessarily imply that

$$\left|\frac{s-s_k}{\Omega}\right| < 1/2.$$

In fact, since the s_k are either real, or occur in conjugate complex pairs, one will generally have to deal with a series of the type $R_m^{(o)}$, but with an argument greater than .5, even if the s_k are smaller than $\frac{1}{2}\Omega$ (small bandwidth assumption). Referring back to the previous paragraph therefore, it is clear that a satisfactory approximation cannot be expected for the entire function unless at least three terms of the original sum, and one term in the expansion of the remainder are included. Remarkably enough, if this type of approximation is adopted for the individual terms, it turns out (see below) that the contribution from the remainder drops out in the final sum.

In order to see this one must first obtain the approximate expression for

$$\sum_{-\infty}^{+\infty} \frac{1}{(s+jn\Omega)^2},$$

which may be obtained directly from that for

$$\sum_{-\infty}^{+\infty} \frac{1}{s+jn\Omega}$$

by differentiation with respect to s. Thus,

$$\sum_{-\infty}^{+\infty} \frac{1}{(s+jn\Omega)^2} = \sum_{-m}^{+m} \frac{1}{(s+jn\Omega)^2} + R_m\tau(0')^i(s), \tag{103}$$

with

$$R_m^{(o')}(s) = +\frac{1}{s^2}\sum_{l=0}^{\infty} 2(2l+1)c(l+1, m)\left(\frac{s}{j\Omega}\right)^{2(l+1)}. \tag{104}$$

Summing (96), (102), and (103) with the appropriate coefficients [as given by (74)] one finds that $R_m(s)$, the total remainder [see (94)] is given as

$$R_m(s) + A(0)R_m^{(o')}(s) + A'^{(0)}R_m(0)(s) + \sum_{k=1}^{n} \frac{a_k}{s_k^2} R_m^{(k)}(s). \tag{105}$$

Inserting the appropriate expressions for $A(0)$ and $A'(0)$ and combining the various terms one finds that

$$R_m(s) = \sum_{l=0}^{\infty} 2c(l+1, m)(j\Omega)^{-2(l+1)}\left[\sum_{1}^{n} \frac{a_k}{s_k^2}(s^{2l+1} - (s-s_k)^{2l+1} - (2l+1)s^{2l}s_k)\right]. \tag{106}$$

The first term in this expression ($l=0$) vanishes, and one thus has the rather remarkable result that the error entailed in approximating the total starred function by finite sum, is precisely that which arises when the remainders $R_m^{(k)}(s)$, etc., are approximated by their first term! The result (4.46) may be put in a more convenient form by introducing the quantities $a_o^{(m)} = \sum a_k s_k^m$ first defined by (78). One then finds that[15]

[15] $\binom{2l+1}{q} = \frac{(2l+1)!}{q!(2l+1-q)!}$.

$$R_m(s) = 2\sum_{l=1}^{\infty} c(l+1, m)(j\Omega)^{-2(l+1)} \sum_{q=0}^{2l-1} \binom{2l+1}{q} a_o^{(2l+1-q)} s^q. \quad (107)$$

In this form $R_m(s)$ is expressed as a series of decreasing powers of Ω (or increasing powers of τ). In particular, for $m=0$,

$$R_o(s) = 2\sum_{l=1}^{\infty} c(l+1, 0)(j\Omega)^{-2(l+1)} \cdot \sum_{q=0}^{2l-1} \binom{2l+1}{q} a_o^{(2l+1-q)} s^q. \quad (108)$$

Inserting the value $c(2, 0)=\pi^4/90$, and the fact that $\Omega=2\pi/\tau$, one finds

$$R_0(s) = \frac{\tau^4}{720}[a_o^{(1)} - sa_o] + \cdots$$

in agreement with (81), the expansion in powers of τ. Eq. (108) thus gives this basic result in a quite explicit form, and (107) allows one to extend the result to the determination of the series expansion, in terms of τ, of the difference between the exact result and the finite sum approximation. The above result may also be expressed more directly as a series in s. In this case,

$$R_m(s) = \frac{2}{j\Omega}\sum_{q=0}^{\infty}\left(\frac{s}{j\Omega}\right)^q \cdot \left[\sum_{l\geqq(q+1)/2}^{\infty} c(l+1, m)\binom{2l+1}{q}(j\cdot\Omega)^{-(2l+1-q)} a_o^{(2l+1-q)}\right]. \quad (109)$$

The above formulas (107) and (109) enable one to estimate the errors involved in various finite term approximations to the starred transfer function. One may obtain a rough estimate directly from (107) by noting the approximation (101) for $c(l+1, m)$ and the fact that $a_o^{(m)} \sim s_c a_o$ where s_c gives the bandwidth of $A(s)$. Inserting these values and completing the sum, one finds that

$$R_m(s) \lesssim \frac{2(s-s_c)^2 a_o}{(s-s_c)^2 + (m+1)^2\Omega^2}. \quad (110)$$

One final remark is in order regarding the above approximations. While the above series will converge more slowly as the bandwidth of $A(s)$ increases (because the $a_o^{(m)}$ increases) no real difficulty will arise as long as $|s_c| < \frac{1}{2}\Omega$. Since the general term in the series is given explicitly it is possible to estimate the error involved at any stage even when the convergence is slow, which is unfortunately not the case for the earlier approximations. These advantages tend to balance the rather cumbersome (i.e. additive) nature of the formulae as compared, say, with (86) or (91).

This section is most fittingly concluded with a brief discussion of the case where τ is rather large or where $A(s)$ is very heavily damped. This is more or less the opposite extreme from that discussed here till now. Returning to (76) one writes

$$\left(\frac{A(s)}{s^2}\right)^* = A(0)\frac{\tau^2}{4}\operatorname{cosech}^2\frac{s\tau}{2} + A'(0)\frac{\tau}{2}\coth\frac{s\tau}{2} + \sum_{1}^{n}\frac{a_k}{s_k^2}\frac{\tau e^{-(s-s_k)\tau}}{1-e^{-(s-s_k)\tau}}.$$

By assumption, $e^{s_k\tau}$ is very small, and hence

$$\left(\frac{A(s)}{s^2}\right)^* \simeq A(0)\frac{\tau^2}{4}\operatorname{cosech}^2\frac{s\tau}{2} + A'(0)\frac{\tau}{2}\coth\frac{s\tau}{2}. \quad (111)$$

Taking $A(0)=1$ $A'(0)=-T$, this becomes

$$\left(\frac{A(s)}{s^2}\right)^* \simeq \frac{\tau^2}{4}\left(\coth^2\frac{s\tau}{2} + \frac{2T}{\tau}\coth\frac{s\tau}{2} - 1\right). \quad (112)$$

The starred transfer function now depends on $A(s)$ only through the time constant T (damping) of the latter. [Related results were obtained by MacColl[1] for $A^*(s)$.]

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I am indebted to Mr. H. Gruen and Mr. J. H. Irving for many interesting and helpful discussions on the above topics. Much of this work was done while the author was at the Hughes Aircraft Company.

Correspondence

On the Input Impedance Network Error in Operational Amplifiers

The problem of the effect of the input impedance of transistors becomes important if these devices are to be used in analog computing circuits. Although it is true that the circuit accuracy will be better for a fixed forward voltage gain if the input impedance is as large as possible, it is of interest to determine just how seriously the transistor limits the accuracy due to its input properties.

Consider the voltage summing amplifier

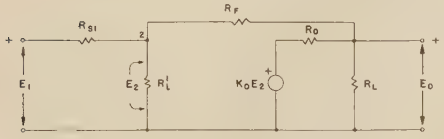

Fig. 1—Parallel feedback circuit.

of the parallel feedback type shown in Fig. 1. The amplifier supplying the forward gain is represented by its input resistance, output resistance, and open circuit voltage gain. E_1 represents one of the applied input voltages, E_0 the output voltage due to E_1, and R_i' is the parallel combination of the other input summing resistances and the input resistance R_i of the active portion of the network. The ideal output for the input E_1 will be called E_0' and is given by

$$E_0' = -\frac{R_f}{R_{s1}} E_1. \tag{1}$$

The forward gain of the amplifier will be defined *with the feedback connected* as K_{0f}

$$K_{0f} = \frac{E_0}{E_2} = \frac{K_0 + \dfrac{R_0}{R_f}}{1 + \left(\dfrac{R_f + R_L}{R_f R_L}\right) R_0}. \tag{2}$$

The error in per cent will be defined by

$$\mathcal{E} = 100\left(\frac{E_0 - E_0'}{E_0'}\right). \tag{3}$$

By writing the node equation at point 2 and making use of (1)–(3) we find the per cent error is

$$\mathcal{E} = \frac{100}{K_{0f}} \cdot \frac{\left(1 + \dfrac{R_f}{R_{s1}} + \dfrac{R_f}{R_i'}\right)}{1 - \dfrac{\left(1 + \dfrac{R_f}{R_{s1}} + \dfrac{R_f}{R_i'}\right)}{K_{0f}}}.$$

Under conditions of good accuracy

$$\frac{\left(1 + \dfrac{R_f}{R_{s1}} + \dfrac{R_f}{R_i}\right)}{|K_{0f}|} \ll 1,$$

so the error equation becomes approximately

$$\mathcal{E} = \frac{100}{K_{0f}}\left(1 + \frac{R_f}{R_{s1}} + \frac{R_f}{R_i'}\right). \tag{4}$$

Eq. (4) is in a form convenient for the substitution of the easily measurable quantities R_i' and K_{0f}. Note that any error due to R_i can be made up by using a larger forward gain. Eq. (4) also indicates that a lower impedance level is desirable in the feedback network for small error if R_i is small. Of course, this cannot be taken to an extreme limit since K_{0f} is somewhat dependent upon R_f through (2).

As an example consider a two-input summing amplifier having a gain of -5, $K_{0f} = -20{,}000$, $R_f = 50\text{K}$, $R_i = 50\text{K}$. This value of R_i is obtainable using a grounded collector input circuit. The value of R_i' is then about 8.4K and the error as computed from (4) is .06 per cent. If R_i were infinite, the error would be .055 per cent.

Another important case of interest is the integrator connection where a capacitor replaces R_f. The error can now be defined in terms of the response to a standard waveform such as a step or in terms of the frequency behavior of the network. The latter representation is most convenient for the application of the error formulas derived above. If we substitute $1/j\omega c$ for R_f in the error equation we see that a low input impedance limits the accuracy at low frequencies which results in long time errors in the integration. Here again a low impedance feedback network is desirable by using as large a value of feedback capacitor as possible.

The above discussion emphasized what may be termed network errors, i.e., errors due to the nonideal values of the network elements in the amplifier. Another very important class of errors are the drift errors which are most often due to changes in the network elements or power supply sources. The problem is most severe in the integrator connection where dc feedback is not available, and the error becomes worse as the time of computation increases. It is standard practice in high quality vacuum tube computers to use chopper stabilization for drift reduction. This technique can be used with the same degree of success in a transistor computer where the drift is primarily due to temperature effects on the transistors.

The above discussion indicates that the input network properties of transistors does not preclude using them in high quality operational amplifiers with accuracies of the same order attainable with vacuum tubes. This requires in general, a low impedance level in the feedback network and a chopper system if high quality integrators are to be constructed.

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Two's Complement Multiplication in Binary Parallel Digital Computers

For a binary computer employing the two's complement representation of negative numbers, the generalization is often made that the hardware required is relatively simple for addition and subtraction, but that circuitry for sequencing multiplication is complicated by the necessity for one or more corrections. With certain minor restrictions, it is possible to perform multiplication without the necessity for a correction.

It is necessary to note the following characteristics of the two's complement system of representation. If a number y in the range $-1 \leqq y < 1$ is represented by a set of $n+1$ binary digits y_i ($i = 0, 1, \cdots, n$), then the algebraic value y is related to the binary digits y_i by the formula

$$y = -y_0 + \sum_{i=1}^{n} 2^{-i} y_i,$$

where $y_0 = 0$ if $y \geqq 0$ and $y_0 = 1$ if $y < 0$. The digit y_0 is the sign digit and indicates the correct sign of y only when y is in the range $-1 \leqq y < 1$. The weighted sum of the nonsign digits is

$$\sum_{i=1}^{n} 2^{-i} y_i = y + y_0,$$

and lies in the range $0 \leqq y + y_0 < 1$.

In essence, the proposed method of forming a product xy of a multiplicand x and a multiplier y, is the following:

1. if $y \geqq 0$, form xy:
2. if $y < 0$, form $(-x)(-y)$.

The assumption is made that the product is formed by a sequence of n steps, n being defined as the number of nonsign digits of the multiplier. Each step involves a sensing of one multiplier digit, a conditional addition of the multiplicand x to a partial product, and a right shift of one digital position. Use of the right shift implies that the least significant digit of the multiplier is sensed first.

Two problems arise in connection with the proposed method of multiplication. (1) In the formation of xy, for example, the formation of a new partial product p_{k+1} from the previous one (p_k) is described by the equation

$$p_{k+1} = 1/2(p_k + y_{n-k}x),$$

where y_{n-k} is the multiplier digit sensed during step k of the process, y_n being the least significant digit. The expression $+y_{n-k}x$ represents the conditional addition of the multiplicand and the factor $1/2$ represents the right shift.

If, in the above equation, x lies in the range $-1 \leqq x < 1$, then p_k is also in the range $-1 \leqq p_k < 1$, with the result that the sum $p_k + y_{n-k}x$ is in the range $-2 \leqq p_k + y_{n-k}x < 2$. The sign digit of the sum may not be a true indication of its algebraic sign, so that special circuitry is necessary to generate the correct sign digit during the right shift which forms p_{k+1}.

The analysis of the problem of forming the correct sign digit for p_{k+1} is relatively simple. If the sign digits of p_k and $y_{n-k}x$

agree, then their sign digit is the correct sign digit for p_{k+1}. If the sign digits of p_k and $y_{n-k}x$ disagree, then the sum $p_k+y_{n-k}x$ lies in the range $-1 \leqq p_k+y_{n-k}x<1$, and the sign digit of the sum is a true indication of its algebraic sign.

(2) A second problem arises when the multiplifier y is negative; it is then necessary to form the two's complement of y. If the digits of y are sensed serially, least significant digit first, then the following complementation rule used in some serial computers can be applied.

"Beginning with the least significant digit, leave the digits of the multiplier unchanged up to and including the first 1, thereafter replace 0's by 1's and 1's by 0's."

The formation of $-x$ presents no difficulty, since complementing facilities are necessary for the subtraction instruction, and may well be connected to the register in which the multiplicand is held during the multiplication. It is therefore possible, when y is negative, to form the product $(-x)(-y)$ by means of a sequence of n conditional subtractions and shifts, n being the number of nonsign digits of the multiplier. The method fails only when the multiplier $y=-1$.

It is interesting to review the methods proposed for two's complement multiplication. The earliest method[1] consisted essentially of forming the product of the nonsign digits of both multiplier y and multiplicand x, which is equivalent to forming

$$(x + x_0)(y + y_0) = xy + x_0y + y_0x + x_0y_0,$$

and which required two corrective steps as well as the addition of the digitwise complement of the multiplier. The problem of sign digit insertion in forming partial products was avoided, since $x+x_0$ and $y+y_0$ are positive, with the result that the partial products p_k are positive.

A method developed for the ORDVAC[2] in November, 1950, requires special circuitry for insertion of the correct sign digit during the right shift, as discussed above. The process is then one of forming, in n steps,

$$x\sum_{i=1}^{n} 2^{-i}y_k = x(y + y_0),$$

and requires a single correction in the form of a subtraction of the multiplicand x if the multiplier is negative.

In both the ORDVAC and the ILLIAC, the circuitry required for sequencing corrective steps is more complicated than the special sensing circuitry required for sign digit correction and for complementing the multiplier. Consequently, the method proposed here could be applied to either of these computers to reduce both the multiplication time and the hardware necessary.

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Contributors

A. S. Hoagland (S'50–A'54) was born in Oakland, California on September 13, 1926. He attended the University of California where he received the B.S., M.S. and Ph.D. degrees in 1947, 1948 and 1954, respectively. During the period 1948–1949, he was employed as an engineer on the California Digital Computer Project (Caldic).

Since 1950, he has been on the staff of the Division of Electrical Engineering at the University of California where he is now an Assistant Professor. He is currently engaged as an engineering consultant by the International Business Machines Corporation Laboratory at San Jose, California.

Dr. Hoagland is a member of Phi Beta Kappa, Sigma Xi, Eta Kappa Nu, Tau Beta Pi, and is an associate member of the AIEE.

Arthur S. Robinson (S'48–A'49) was born in New York City on September 26, 1925. He received the B.S. degree in electrical engineering from Columbia University in 1948, and the M.E.E. degree from New York University in 1951.

In 1948 Mr. Robinson joined Hazeltine Electronics Corporation, where he worked on video and pulse circuitry, precision test test equipment and radar and IFF systems. In 1951 he became associated with the W. L. Maxson Corporation, working on display and computing techniques. In 1952 he joined the Columbia University Electronics Research Laboratories, where he has served as a Group Leader in the computer and control system fields. His current work is in the application of analog and digital computing techniques to control systems and real time data processing problems.

Mr. Robinson is a member of Tau Beta Pi.

F. S. Preston was born in Iowa City, Iowa, June 30, 1918. He received the B.S. degree in electrical engineering at the University of Washington in 1940 and the M.S. degree in electrical engineering at the Massachusetts Institute of Technology in 1942. He was a staff member in the Electrical Engineering Department of MIT during 1941 and a research associate in the High Voltage Laboratory of MIT during 1942–1943. Since 1944 he has been with the Norden Laboratories, White Plains, New York. He is now Assistant Director of Engineering and Project Engineer with Norden, where he has worked on uhf, the design of electrical analog computers, development of digital devices and development of systems and instruments for military airborne use.

Mr. Preston is a member of the IRE, Vice-Chairman of the Westchester Sub-section of the New York IRE, a member of the Association for Computing Machinery, Tau Beta Pi, and Sigma Xi.

T. Teichmann was born in Königsberg, Germany in 1923. He received the B.Sc. degree (Electrical Engineering) in 1943 and the M.Sc. degree (Mathematics) in 1945 from the University of Cape Town. He received the M.A. degree in 1947 and the Ph.D. degree (Physics) in 1949 from Princeton University. His graduate work was in theoretical nuclear physics.

Dr. Teichmann was a Lecturer in Electrical Engineering from 1944 to 1946 and a Research Associate from 1950 to 1952 at Princeton University. His work at Princeton University included theoretical work on nuclear reactions and scattering, electromagnetic accelerators and microwave junctions. Dr. Teichmann was a Research Physicist with the Research and Development Laboratories of the Hughes Aircraft Company during 1952–1955 where he worked on fire control systems and operations research. Dr. Teichmann is now with the Research Laboratories Branch of the Missile Systems Division of Lockheed Aircraft Corporation.

PGEC News

Message from the New Chairman

The traditional result of taking over the Chairmanship of an organization is that the new man finds that the membership is dwindling and that the only thing lower than the enthusiasm of the remaining membership is the balance in the Treasury. It is an honor to become Chairman of the PGEC where none of these things are true. Our membership is expanding rapidly. We are the largest group in the Institute of Radio Engineers. One out of every 12 members of the IRE belongs to our group. The attendance at our conferences and meetings strains the largest facilities that we can provide. Our Treasury is suffering from an embarrassment of riches. Obviously the previous administration of our group has been excellent. I hope to be able to contribute to the maintenance of the good health of our organization. The only thing I can find to complain about is that our membership, so lively and vocal at conferences and meetings, seems strangely silent in between the big shows. Those of us who have responsibilities for the operation of the group hope that as long as the group continues to grow it is not suffering seriously from mismanagement. There must, however, be some measure of success other than growth. We are anxious to obtain more backtalk from the membership. We want to know what we should be doing as well as how we are doing. I would appreciate private correspondence on the

affairs of the group but I suggest that we use the Letters to the Editor Department of the Transactions as the error detection and correction circuit essential to every computer and, I believe, computer organization.

* * *

Every year the terms of five of the members of the PGEC Administrative Committee expire. Every year, ten candidates for the five committee memberships are proposed by a nominating committee whose chairman is the chairman of the previous year's Administrative Committee. This committee works with the chapters in order to see that active and capable candidates are nominated. The details of this cooperation are defined in the By-Laws of our PGEC Constitution which is printed in this issue of the Transactions.

In order to provide a maximum of democracy, without encouraging confusion, means are also provided for members of the Group to nominate candidates directly. A petition signed by 25 members will result in their candidate being nominated for the Administrative Committee. I wish to remind all our members of this opportunity to take a very direct part in the affairs of the Group. Nominations will be accepted until February 20, 1956.

—J. H. Felker, Chairman

Nomination for New PGEC Administrative Committee Members

The PGEC Administrative Committee is composed of 15 members, each serving 3 years. The terms are overlapped in such a way that 5 new members are elected each year. Nominations come from two sources. One source is a Nominations Committee composed of several members of the Administrative Committee and several Chapter chairmen. The other source is nomination by petition from the general membership. You are hereby notified that nominations are now open for the 5 new PGEC Administrative Committee members to serve from April, 1956, through March, 1959. Nomination petitions must be supported by the legible signatures of 25 members of the PGEC. Nominations close February 15, 1956. Please forward your nominations to Harry T. Larson, Chairman, Nominations Committee, The Ramo-Wooldridge Corporation, 5740 Arbor Vitae, Los Angeles 45, California.

Annual ACM Meeting

The annual meeting of the Association for Computing Machinery will be held at the University of Pennsylvania in Philadelphia on September 14–16, 1955. The topics to be covered in the sessions at the meeting include the following:

Analog Computers
Numerical Analysis
Business Applications of Computers
Logical Algebra
Logical Design of Computers
Recent Systems Developments
Statistical Applications
Advanced Programming Techniques
Linear Programming Applications
Sorting Methods
Data Processing Techniques
Digital Computer Component Development

Eastern Computers Conference

The Eastern Computer Conference sponsored jointly by the IRE, ACM, and AIEE will be held at the Hotel Statler in Boston on November 7–9, 1955. The theme of the conference is "Computers in Business and Industrial Systems." Mr. John S. Coleman, President of Burroughs Corporation, will provide the introductory address and Dr. J. D. Brainerd, Chairman of the Electrical Engineering Department of the University of Pennsylvania and General Chairman of the Conference will be the keynote speaker during the opening session. A tentative list of topics to be covered at the meeting is as follows:

Monday afternoon:
"Role of Computers in Business"
Tuesday morning:
"Unit Records versus Tape Records in the Electronic Accounting Systems"
Tuesday afternoon:
"Trends in Systems Design"
Wednesday morning:
"Standardization in Electronic Computers," including a panel discussion on problems in magnetic tape standardization

Dr. Irvin Travis is Program Chairman for the meeting. Information concerning registration may be obtained from Mr. Jack Porter, Local Arrangements Committee, Digital Computer Laboratory, Massachusetts Institute of Technology.

National Simulation Conference

The Dallas-Fort Worth Chapter of the Institute of Radio Engineers Professional Group on Electronic Computers (PGEC) will sponsor a National Simulation Conference in Dallas, Texas, on 19–21 January 1956.

The Conference will be devoted to simulation and associated computing techniques, and will include topics in (1) general simulation (mathematical, physical, logistic, etc.); (2) advances in computer design, techniques, and applications, and (3) methods of determining and improving the accuracy of analog solutions.

Papers to be presented at the Conference are hereby solicited. Although it is expected that most of the papers will deal with analog computers, papers on the use of digital computers in simulation are strongly encouraged.

Western Computer Conference

The Western Computer Conference will be held in San Francisco, February 8, 9, 10, 1956. It is sponsored jointly by the AIEE, IRE, and ACM.

Papers on all phases of the computer field are now being solicited. In addition to the title, authors are asked to submit an abstract of approximately 200 words, suitable for reproduction in the program, and either the complete manuscript or sufficient additional information to permit evaluation by the Technical Program Committee. Early submission of papers is desired, the final deadline being November 15. This is the latest date that is operationally feasible and papers received thereafter cannot be considered.

Authors should indicate any plans for publication and should state what facilities, such as slide or movie projectors, power sources, etc., are required. For uniformity of handling, it is requested that all papers be directed to: Byron J. Bennett, Chairman, Technical Program Committee, Stanford Research Institute, Menlo Park, California.

International Computer Conference

An international conference on electronic digital computers and data processing will be held at the Institute für Praktische Mathematik, Technische Hochschule, Darmstadt, Germany on October 25–27, 1955. The conference is sponsored jointly by the Gesellschaft für Angervandte Mathematik und Mechanik and the Nachrichtentechnische Gesellschaft im Verband Deutscher Elektrotechniker. Information on registration may be obtained by writing to: Prof Dr. A. Walther, Technische Hochschule, Institut für Praktische Mathematik, Darmstadt, Germany.

New Appointments in PGEC

R. C. Matlack, Bell Telephone Laboratories, Inc., 463 West Street, New York, 14, New York has been appointed as the new Secretary-Treasurer of the IRE-PGEC. An additional appointment which has been announced by J. H. Felker, Chairman of the PGEC is that of Dr. J. P. Eckert, Jr., Director of Engineering, Remington Rand, Inc., 2300 West Allegheny Avenue, Philadelphia 29, Pa., as the Chairman of the Awards Committee.

New Officers of Los Angeles Chapter of PGEC

The new officers (effective September 1, 1955) of the Los Angeles Chapter of the Professional Group on Electronic Computers are Roger Sisson, of Canning, Sisson Associates, 914 S. Robertson Boulevard, Los Angeles 35, California who is Chairman; William Speer, of the National Cash Register Company, 3348 W. El Segundo Boulevard, Hawthorne, California, who is Vice Chairman; Keith W. Uncapher, of The RAND Corporation, 1700 Main Street, Santa Monica, California, who is Secretary; William Arsenault, of the Magnavox Research Laboratories, 2255 Carmelina Ave., Los Angeles 64, California, who became Treasurer; and John Alrich, of the ElectroData Corporation, 717 North Lake Street, Pasadena 8, California, who was named to the Administrative Committee along with George Gourrich, of the Telecomputing Corporation, 12838 Saticoy Street, North Hollywood, California.

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Reviews of Current Literature

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. Authors can be of considerable assistance in this review process by sending two reprints of their articles to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.—*H. D. Huskey,*

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Bibliography on Ultrasonic Delay Lines—M. D. Fagen. (*Trans. IRE*, vol. PGUE-2, pp. 3–8; November, 1954.) 78 references are listed.

Courtesy of *Proc. IRE* and *Wireless Engineer*

55-78

Computers and Automation—Reference Information.—(*Computers and Automation*, vol. 4, pp. 15–29, 32–46; April, 1955.) The following lists and abstracts appear in this issue: (1) Association for Computing Machinery, Ann Arbor Meeting, June, 1954—Titles of Papers and Abstracts; (2) Western Computer Conference and Exhibit, Los Angeles, March 1–3, 1955—Titles of Papers and Abstracts; (3) List of Products and Services in the Computer Field (Cumulative, 64 entries); (4) Roster of Automatic Computers (Supplement list, 15 entries); (5) Patents in the Computer Field (Jan. 25, 1955 through Feb. 15, 1955, 13 entries).

Gordon Morrison

55-79

Digital Techniques in Analog Systems—M. A. Meyer. (*Trans. IRE*, vol. EC-3, pp. 23–29; June, 1954.) The author describes a computer technique in which pulse rate is used to represent number magnitude. The paper gives a brief discussion of the units needed to mechanize the basic operations: addition, subtraction, multiplication, and integration. Feedback loops can be used to mechanize other operations, such as division. The author demonstrates that computation based on analog computer methods can be performed by proper interconnection of the basic units. The devices needed and described are (1) encoders and decoders, (2) gates and buffers, (3) binary rate multipliers, (4) forward-backward registers, (5) synchronizers and timing generators, (6) diode function generating matrices. Examples of the use of the new computer technique include (1) solution of an ordinary differential equation, (2) solution of a trigonometric equation, (3) autocorrelation, and (4) a digital servo. Although the author claims that "the accuracy of over-all computation can be arbitrarily set to be limited only by the conversion devices," the reviewer believes this to apply only to the precision. The reviewer also deplores the absence of a single reference to any of the "several known techniques" for mechanizing the units needed for the basic operations.

Morris Rubinoff

55-80

Methods Used to Improve Reliability in Military Electronics Equipment—L. D. Whitelock. (*Proc. Eastern Computer Conf., Joint IRE-AIEE-ACM, December 8–10, 1953, Washington, D. C.*, pp. 31–33; 1954). The dramatic growth in size and complexity of military electronic equipment is shown by the number of electronic tubes used on a destroyer: 60 in 1937, 850 in 1944, and 3,200 in 1952. Task Forces organized by the Department of Defense analyzed equipment failures, and attributed them to vacuum tubes in 60 to 70 per cent of the cases, engineering in 10 to 15 per cent of the cases, and components in about 10 per cent. This analysis was in part responsible for a "reliable vacuum tube program," and a "reliable component program" as well as others. Specific recommendations are referenced in the documents, "General Specifications for Electronic Equipment," Naval Ship and Shore, MIL-E-16400 (ships), May 1, 1953, and in "Electronic Applications Reliability Review," published by the Radio-Electronics-Television Manufacturers Association.

Ralph J. Slutz

55-81

Quarterly Report No. 6, Second Series—J. R. Bowman, F. A. Schwertz, *et al.* (*Quart. Rept. Computer Components Fellowship Mellon Inst.*, 92 pp.; January 1, 1955 to March 31, 1955.) This report contains a Part I, "Techniques for Circuit Fabrication," and a Part II, "Electro-Optical Devices." Part I is concerned with the problems of materializing conductors, resistors, capacitors, and inductors on glass surfaces for the purpose of forming circuits that are stable above 200° C. Xerographic printing with or without a subsequent etching technique has been used successfully. Using a vacuum evaporated silicon monoxide dielectric, excellent capacitors have been formed on glass. A photoresist-etching process has been used to solve the problem of fabricating intricately shaped masks required in this work. Part II is concerned with the brightness-voltage-frequency relations of a number of dielectric embedded, and chemically deposited electroluminescent phosphors. Also described is some preliminary work on photoconductive cadmium sulfide films. Finally an account is given of a neon diode which is made to count pulsed radio frequency energy.

A. Milch

55-82

Efficient Linkage of Graphical Data with Digital Computers—E. D. Lucas, Jr. (*Proc. WESCON Computer Sessions, August 25–27, 1954, Los Angeles, Calif.*, pp. 32–37; 1955.) A rather rambling discourse describes a few of the available oscillograph record and film data reducing equipments in general terms. Incomplete mention is made of some analog to digital converters *per se*. Basic operating principles and necessary caveats are omitted.

William F. Gunning

55-83

Automatic Strain-Gage and Thermocouple Recording on Punched Cards—Richmond Perley. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 36–43; January, 1954.) A system designed to automatize the recording of quasi-static data from a jet engine test stand is described in this article. Temperatures and pressures are measured with thermocouples and strain-gage pickups. The analog voltage outputs of these instruments are fed into an analog-to-digital converter. The subtraction of standard voltages in known ratios from the analog voltages and comparison of the remainder with zero is the method employed in the conversion. The resulting 3-decimal-digit data samples are transferred to relay storage units. Two pairs of these are utilized. Two successive data samples are loaded into one pair. These two samples are punched on IBM cards while the other pair of storage units are being loaded with the next two data samples. The data in the second pair is then punched and the first pair loaded, etc. Two hundred samples per minute are punched. A resolution and accuracy of $\pm.1$ per cent of full scale is claimed. A system for commutating the output of the strain gages, thermocouples, and calibration voltage is described. In addition to data samples, each card is automatically punched with information identifying the source of the data. A manual keyboard is provided for entering data, run numbers, etc., into the cards. This system is most useful for those applications that require the recording of many repetitive measurements at a relatively low sampling rate.

Kenneth L. Austin

55-84

Multi-Channel Analog-Digital Conversion System for D-C Voltages—W. S. Shockency. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1954, Los Angeles, Calif.*, pp. 113–117; April, 1954.) This is a resume of a conventional analog-digital converter system, the analog being a relatively

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—*The Editor*

high impedance 100v dc source and the digital form being eight digit binary. The basic scheme for conversion from analog to digits is a well-known successive trial-and-error method. A comparison analog is built up by the successive addition of quantized blocks (of voltage or current) which are proportional to magnitudes of related digits. A block is added to the partial sum; the analog (voltage or current) thereby obtained is compared with the test analog, and the particular block is then retained or rejected as determined by this comparison. Blocks are added and tested in a descending order of magnitude. Completion of the process through the lowest-order increment yields a comparison analog digitized to the system's resolution. The reversal of the system to produce an analog output from a digital input is fairly obvious. Achievement and merit of design would appear to lie in packaging for airborne use, in 32 channel multiplexing means, and in stability and reliability of operation, rather than in novelty of concept. One detects (in the latter part of the article) that the real meat and interest of the project may have been in the details of circuit design, but this subject is treated cursorily and, to many, too incompletely to be of real value.

W. D. Caldwell

55-85

Logic, Discovery, and the Foundations of Computing Machinery—M. E. Maron. (TRANS. IRE, vol. EC-3, pp. 2–7; June, 1954.) This paper begins with the accepted premise that automatic computers are syntax machines; i.e., that they perform logical manipulations on expressions of a formal "language." Definitions for, and relations between, the primitive and defined symbols, primitive and defined operations, meaningful expressions, formation rules, and transformation rules of a formal or synthetic language are given. The interpretation of the computer program as a properly ordered list of the transformation rules of the computer's language establishes a correspondence with synthetic-language concepts which allows their application to computer philosophy. With this correspondence in mind, an analysis is made of the fundamental problems of applying deductive and inductive logic towards meaningful ends within a formal system. It is shown that only for the problem of verifying a given deductive proof can a mechanical procedure be determined; that common experience shows that meaningful theorems and hypotheses are not discovered by any mechanical process, and modern logicians have proved that no "decision method" exists in "higher" languages (e.g. arithmetic) for mechanically establishing the proof of a given theorem. Discovery, which for humans is a matter of intuition and creative ability, is stated as necessary for all but the verification of a deductive proof. The author feels that this ability can be simulated in a machine to some degree by a combination of random generation of hypotheses and subsequent testing against known data. As a conclusion it is claimed that, although a machine's method might be different, it could theoretically accomplish any information manipulation of which a man is capable.

Douglas C. Engelbart

681.142 55-86

Algebraic Method of Synthesis of Multicontact Relay Systems—V. I. Shestakov. (*Compt. Rend. Acad. Sci. (URSS)*, vol. 99, pp. 987–990; December 21, 1954. In Russian.) A vector-algebraic method of synthesis of switching circuits suitable for computers is developed theoretically.

Courtesy of PROC. IRE and *Wireless Engineer*

55-87

The Use of a Reflected Code in Digital Control Systems—F. A. Foss. (TRANS. IRE, vol. EC-3, pp. 1–6; December, 1954.) The reflected (Gray) binary code is described, and relationships between the reflected binary code and the conventional binary code are given. The advantage of the reflected code for use in dynamic parallel readout systems is stated. A relay reflected-to-conventional binary translator is described. Two reflected binary-to-analog converters are described. One of these presents a constant impedance to the power supply, while the other presents a constant impedance to the load. Both of these converters are built of relays and resistors. Using these devices as building blocks, the author proceeds to synthesize several practical devices. The first of these is a digital positional servo which can also be used as an analog-to-digital converter. A digital contactor positional servo is then described, including features which solve a special stability problem encountered at one position of the output shaft. Finally, an accumulator is described which adds a conventional binary number to a reflected binary number which is a function of an angular shaft position.

Harry T. Larson

55-88

Marginal Checking—J. Melvin Jones. (*Computers and Automation*, vol. 4, pp. 10–14; April, 1955.) The concept of marginal checking as a method of preventive maintenance is summarized at an elementary level. Types of failures detected, the methods of their detection, and the criteria for test performance are reviewed. In addition, divisions of the computer into functional groups for marginal checking is proposed as an aid in locating the cause of failure.

Gordon Morrison

ANALOG COMPONENT RESEARCH

55-89

A Wide-Band Square-Law Computing Amplifier—Aaron S. Soltes. (TRANS. IRE, vol. EC-3, pp. 37–41; June, 1954.) This paper describes an amplifier for use on a 40-mcps pulsed carrier. The pulses may be as short as 0.5 microsecond. Output amplitude is proportional to the square of the input amplitude; i.e., $E_{out}=KE_{in}^2$. Bandwidth is 5 mcps at 40 mcps, and accuracy is 1 per cent of full scale over a range of 40 db. A special cathode-ray tube with a parabolic mask is the squaring element. It generates a thin, rectangular beam that is deflected across the parabolic mask. Beam current intercepted by the mask is, then, proportional to the deflection. In the particular arrangement described, the incoming 40-mcps signal is heterodyned down to 20 mcps, and the second harmonic in the output of the squaring element is extracted and amplified. Means for improving the useful dynamic range of the square-law amplifier are suggested.

Stanley Rogers

55-90

A Stabilized Driftless Analog Integrator—Howard Hamer. (TRANS. IRE, vol. EC-3, pp. 19–20; December, 1954.) Although conventional chopper-stabilization reduces integrator output drift due to amplifier unbalance, it does not reduce drift due to input current. Author describes disadvantages of common techniques for input current drift reduction, then shows new chopper-stabilized integrator circuit which reduces drift due to all active components. New circuit simply adds a new resistor and capacitor of RC equal to existing RC, and takes input to chopper from junction of these new elements connected in bridge circuit with existing elements. Theory shows new circuit reduces output drift due to input current by gain of stabilization amplifier. Experimental verification shown.

Walter W. Soroka

ANALOG EQUIPMENT

55-91

A Desk-Model Electronic Analog Computer—M. W. Fossier and H. A. Rosen. (TRANS. IRE, vol. EC-3, pp. 20–24; December, 1954.) A small electronic computer of moderate accuracy (5 per cent) with a frequency range from zero to about 100 cps. The basic components are nine computing amplifiers. The limited nonlinear components are a motor driven potentiometer and two bias voltages. Problems are set up on fiber glass plug boards by wiring linear components and diodes to the board. Particular emphasis is made of the use of transfer functions for economy of computing amplifiers, and passive networks without amplifiers to expand problem solving capacity. It is suggested that this small computer could be used for the relatively less complicated problems arising in a research department and thus not tie up an expensive computer for the purpose. It is also suggested that the computer be used in technical schools for problem solution and the teaching of analog techniques.

Cyril P. Atkinson

681.142 55-92

Australian Guided Weapons Analog Computer—(*Aust. Jour. Instr. Tech.*, vol. 10, pp. 145–146; November, 1954.) Brief description of AGWAC, whose design is based on that of the Royal Aircraft Establishment simulator TRIDAC. The equipment is built up of 280 plug-in units ("bricks").

Courtesy of PROC. IRE and *Wireless Engineer*

681.142 55-93

Differential Analyzer: the N. P. L.'s New Analogue Computer for Solving Differential Equations—(*Engineering (London)*, vol. 178, pp. 659–660; November 19, 1954.) Brief description of a large analyzer, recently brought into use. The machine is

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actuated by a motor driven shaft representing the independent variable. The three principal types of mechanism used are integrators, gear trains and differential gears. Function tables permit an arbitrary function of any variable to be inserted from the graph and also allow solutions to be obtained in graphical form. Setting-up time is low, since all units are coupled by means of servomechanisms which may be connected in any combination through a telephone-type switchboard.

Courtesy of PROC. IRE
and *Wireless Engineer*

681.142 55-94

An Autocorrelogram Computer—G. Revesz. (*Jour. Sci. Instr.*, vol. 31, pp. 406–410; November, 1954.) A comparatively simple and inexpensive instrument is described, with detailed circuit diagram. The signal, recorded on a magnetic tape, is played back through two separate heads, thus producing the functions $f(t)$ and $f(t-\tau)$. These are amplified, multiplied and then integrated by a modified dc watthour meter. The computer was originally developed as a yarn cross-section analyzer.

Courtesy of PROC. IRE
and *Wireless Engineer*

55-95

A One-Dimensional Fourier Analog Computer—Leonid V. Azaroff. (*Rev. Sci. Instr.*, vol. 25, No. 3, pp. 471–477; May, 1954.) The purpose of the instrument described in this paper is to sum

$$\sum_{n=0}^{N} F_n \begin{Bmatrix} \sin \\ \cos \end{Bmatrix} 2\pi nx$$

electrically; N may go up to 30. The sums are given as voltages depending on x, which is essentially time. The sines and cosines are generated by resolvers (a special kind of transformer) whose shafts are connected by a gear train in which the gear ratios are such as to give the harmonics of the Fourier series; that is, the nth primary rotates at angular velocity $n\Omega$ for some preassigned Ω. The input voltages to the primaries are set by variacs at the constant values A_n. When the outputs of the resolvers are appropriately coupled, the machine produces voltages proportional to

$$\sum_{n=0}^{N} A_n \cos 2\pi nx$$

and

$$\sum_{n=0}^{N} A_n \sin 2\pi nx,$$

where N is the number of harmonics and x is the dimensionless quantity $\Omega t/2\pi$. It is immaterial how specific values of x are identified; the interest is in measuring the sum at a sufficient number of points of a period: 0 to 1 on 0 x, to $2\pi/\Omega$ on t.

Stanley Katz

UTILIZATION OF ANALOG EQUIPMENT

55-96

An Electronic Differential Analyzer as a Difference Analyzer—Louis B. Wadel. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 128–136; July, 1954). Methods are discussed for utilizing an electronic differential analyzer as a difference analyzer (1) to solve ordinary difference equations and (2) to solve ordinary differential equations by related difference equations. It is stated that the digital "differential" analyzer is improperly named and should be called a digital "difference" analyzer since these devices are basically designed on difference equation principles. Such analyzers are able to solve ordinary differential equations by virtue of a single method of approximate integration which utilizes a difference equation and is included in the device as a built-in program. The following equation is given as an example for describing the setup and operation of an electronic differential analyzer to solve difference equations:

$$E^3X + 0.6E^2X + 0.4EX + 0.5X = 20.$$

Six integrators are required for the solution with the operate and hold controls on three of the integrators operated in reverse sequence of those on the other three integrators. The iteration process required is controlled by a timing mechanism operating the respective groups of integrators in sequence. Although only linear difference equations are discussed, the author states that nonlinear difference equations could be solved by utilizing standard electronic differential analyzer techniques for introducing nonlinearities into the equations. The following equation is used in describing the use of an electronic differential analyzer as a difference analyzer for solving ordinary differential equations:

$$\dddot{X} + .02\ddot{X} + .0025X = 0.$$

The difference equation utilized for the approximate integration method employed is

$$X(t+h) = X(t) + h\ddot{X}(t)$$
$$\ddot{X}(t+h) = \ddot{X}(t) + h\dddot{X}(t).$$

Four integrators are required in the solution but two of these are utilized as integrators and the other two as storage elements. A sequencing device controls the condition of the integrators by a program established by the iteration method. Although this method of solving a differential equation requires more integrators than the normal method for utilizing electronic differential analyzers, it has the possibility of utilizing multiplexing techniques to reduce the number of integrators required in more complex problems. In conclusion, it is noted that with the exception of the control circuitry no special equipment is required to use an electronic differential analyzer in the ways described.

Charles M. Edwards

55-97

Analog Study of Electron Trajectories—Benjamin F. Logan, George R. Welti, and George C. Sponsler. (*Jour. Assoc. Comp. Mach.*, vol. 2, pp. 28–41; January, 1955.) This paper describes the study of electron trajectories by means of the analog computer at the Dynamic Analysis and Control Laboratory at MIT. Field information derived from a model electrode system in an electrolytic tank is given as a function of the co-ordinates continuously and automatically to the computer when the equations of electron motion are integrated and plotted. The field measuring errors introduced by the probe, the correction and calibration techniques are given in detail. A complete list of references is given at the end of the article.

J. C. Chu

DIGITAL COMPONENT RESEARCH

55-98

Transistor Circuitry for Digital Computers—C. L. Wanlass. (TRANS. IRE, vol. EC-4, pp. 11–16; March, 1955.) Three different types of circuit are described: a direct-coupled flip-flop, a novel arrangement of diode gates, and a "write" amplifier for a magnetic disc. These circuits, operable at frequencies to 200 kc, utilize junction transistors which are allowed to saturate. The flip-flop is a transistor equivalent of the familiar Eccles-Jordan circuit, with a single power supply and a common emitter resistor. Output amplifiers which are parallel combinations of two common-collector circuits (one *n-p-n* unit and one *p-n-p* unit) enable the flip-flop to drive the logic circuits with current of either polarity with equal facility. A shunt output capacitor is used to store energy. The number of parallel loads which the flip-flop can drive is then a function of the size of this capacitor and the characteristics of the clock. Up to 300 loads have been driven successfully at 50 kc. As many as four stages of the "dc pulse" logic gates are feasible in an "and-or-and-or" configuration. An unusual feature of the logic circuitry is that only a single "pull-down" resistor is needed for the four tandem stages, reducing considerably the attenuation in the logic circuitry. A disadvantage of this feature is that a 0 signal at one input to an "and" circuit pulls down the output points of preceding logic stages. This prevents driving several parallel inputs from the output of a two or three stage logic circuit. The magnetic disc write amplifier is a modification of the flip-flop circuit. Current always flows in the write winding in one direction or the other, depending upon the flip-flop state. Such an arrangement is not convenient for a conventional computer, in which no information is written during considerable periods of time, but is ideally suited for the differential analyzer application for which it was intended. Detailed circuit schematics and information about tolerable component variations are included in the article.

R. A. Kudlich

55-99

Transistor Flip-Flops for High-Speed Computer Applications—Edmond U. Cohler. (*Proc. WESCON Computer Sessions, August 25–27, 1954, Los Angeles, Calif.*, pp. 38–43; 1955).—The paper describes and lists capability ranges of several transistor flip-flop designs. Most emphasized are symmetric circuits using two point contact transistors. Static design is based upon the emitter input characteristic in the form of a composite N-curve. By choice of proper emitter impedances, saturating or non-saturating circuitry is obtained. The former has more constant output level and freedom from noise problems; the latter a two to one speed advantage. Capacitor, transformer and steering circuit coupling methods are discussed. Mentioned briefly are clamped,

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ngle transistor flip-flops of the "current" ype. Their advantages of component sav- ng, power and cost are offset by smaller oise margins, greater difficulties in obtain- ng a complementing input, and the lack of ual outputs. Junction transistor flip-flops ith comparable output and input character- stics, but one-third to one-tenth the mega- ycle repetition rates of point contact ransistor flip-flops are reported.

Reviewer's Note: Flip-flop designs capa- le of megacycle rates are possible with the ew high speed junction transistors now vailable. Speed, trigger, and output ranges re summarized. Application in a counter nd checking circuit using 48 transistors are ited.

E. E. Sumner

537.227 55-100

Ferroelectric Properties of Single Crys- als—C. F. Oxbrow. (*Nature (London)*, vol. 174, pp. 1091–1093; December 11, 1954.) Report of a colloquim held at Christchurch, England, in September, 1954.

Courtesy of Proc. IRE and *Wireless Engineer*

621.385.832.681.142 55-101

The Physics of Cathode-Ray Storage Tubes—C. N. W. Litting. (*Jour. Sci. Instr.*, vol. 31, pp. 351–356; October, 1954.) A non- mathematical account is given of the princi- al theories of the cr-storage-tube mecha- ism and of experiments made to test these heories. Theory based on the triode tube xplains the experimental results obtained t Manchester and also explains the con- inued usefulness of the original theory of Williams and Hilburn.

Courtesy of Proc. IRE and *Wireless Engineer*

55-102

Pulse Responses of Ferrite Memory Cores—James Robert Freeman. (*Proc. WESCON Computer Sessions, August 25–27, 1954, Los Angeles, Calif.*, pp. 50–61; 1955.) This paper considers the pulse responses that may be expected from ferrite cores in a coincident current memory with a two-to- one current selection system. The various pulse sequences which may occur in such a memory system are tabulated and the out- puts for each possible pulse sequence are thoroughly analyzed. These outputs are divided into reversible and irreversible com- ponents. Data is presented on amplitudes and waveforms covering all the possible pulse conditions for samples of General Ceramics and Steatite Corp. s-1 material. The effect of overdriving the memory cores is also considered. A brief consideration of the cummulative effects of the core outputs as used in a memory system is made with a figure of merit derived for the memory. The article is very complete in its coverage of the possible situations arising in a coincident current memory. However, further informa- tion on the core behavior in following various paths around the hysteresis loop would help clarify some of the detailed explanation. The information presented should be very helpful in the study, evaluation, and testing of fer- rite cores for use in coincident current mem- ories.

R. B. Arndt

537.227: 546.431.824—31+547.476.3 55-103

Ferroelectric Ceramic with Very Pro- nounced Nonlinear Properties—T. N. Ver- bitskaya. (*Comp. Rend. Acad. Sci. (URSS)*, vol. 100, pp. 29–32; January 1, 1955. In Russian.) A comparison is made of the varia- tion of the dielectric constant with applied electric field for Rochelle salt, $BaTiO_3$, T-7500, and Varikond VK-1. The last- mentioned is similar to Rochelle salt in re- spect of the large change of the dielectric constant in fields up to 1 kv/cm. Experi- mental results are presented graphically.

Courtesy of Proc. IRE and *Wireless Engineer*

55-104

Digital Computer Plug-In Units and As- sociated Equipment—J. N. Harris and F. L. McNamara. (*Elec. Eng.*, vol. 74, pp. 326–329; April, 1955.) A line of plug-in units for digital computer systems is described, plus rack equipment and power supply equip- ment designed for the plug-ins. The units include flip-flops, delay line, general-purpose diode matrix, gates, cathode followers, buffer-inverters, pulse generators, blocking oscillators, etc. The most used tube types are 5965, 5687, and 7AK7. Conservative design has been employed, allowing for in- dividual voltage variations of ± 10 per cent and, in many cases, allowing for "considera- ble deterioration" of the transconductance before the operation of a circuit is impaired. Circuits require six voltages. The power supply equipment and wiring allow a marginal testing power supply to be switched series with any other power supply, making it possible to vary the nominal voltage ± 100 volts. Some mechanical, power, and cooling characteristics are given. No circuit dia- grams are included.

Harry T. Larson

DIGITAL SYSTEMS RESEARCH

55-105

On Single vs Triple Address Computing Machines—Calvin C. Elgot (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 119–123; July, 1954.) Users of computing machines with single-address and three-address have often discussed the "efficiency" of the two types of instruction techniques. Despite much talk and "intuition" on the parts of proponents of each, no final decision has obviously been reached. The author, in this theoretical study, proves that for arithmetic operations only, under simplifying assumptions about the two logics, a "simplified single-address machine" is at least as good as a "simplified three-address machine" as far as instruction storage efficiency is concerned. The simpli- fied three-address machine is assumed simi- lar to the EDVAC-type computer; the simplified single-address instruction ma- chine similar to a Princeton-type computer, but with "inverse subtraction" and "inverse division" allowing direct computation with the three-address logic. With this logic, the single-address machine proves from 12:11 down to 12:7 times as efficient in instruction storage. It is interesting to note that despite this study, made in connection with a de- cision as to the logic of the NORC, that machine was finally designed with three- address instruction stored one to a word, rather than two single-address instructions stored per word.

John W. Carr, III

DIGITAL EQUIPMENT

55-106

System Specifications for the DYSEAC—Alan L. Leiner. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 57–81; April, 1954.) The DYSEAC was developed by the National Bureau of Standards to provide a high capacity general purpose computer having extreme input-output flexibility. The com- puter is intended to work in a real time en- vironment requiring communication with and control of external devices, including other computers. In general, the input-out- put flexibility is based on three properties. First, in-out and computing are simultane- ous and independent. Second, program con- trol can be co-ordinated automatically with the in-out operations, eliminating synchro- nizing problems. Third, special operations for program control and monitoring can be controlled manually or from external de- vices. The paper describes the system logic, which clearly shows its SEAC inheritance. The instructions and program control are described. The rather bewildering array of interlocks, externally initiated program jumps, and other special operations which provide the flexibility mentioned are de- scribed. Particular emphasis is given to the use of two counters for program sequencing which, combined with special instructions, allows the use of relative addresses in pro- gramming, as well as arbitrary jumping be- tween program sequences.

M. M. Astrahan

55-107

Electronic Processing of Air-Traffic- Control Information—R. M. Kalb. (*Elec. Eng.*, vol. 74, pp. 374–377; May, 1955.) This article gives a general description of a system which handles air-traffic flight plans and weather reports. Information pertinent to a given geographic control zone is automati- cally routed to a storage and control unit for that zone. Information on pertinent flights is automatically presented to a human con- troller when the time for his action ap- proaches, and such information is available on demand. Weather reports are received and delivered automatically. The message routing, not described in this paper, is ac- complished on a modified 81D1 system. The over-all characteristics of the magnetic drum storage system are given.

Harry T. Larson

55-108

The Model II Unityper—Louis D. Wilson and Saul Meyer. (Trans. IRE, vol. EC-2, pp. 19–27; December, 1953.) The Unityper is the keyboard input device used to record data on magnetic tape for entry into the Univac. Model I was fundamentally an electronic system, whereas Model II is electromechanical, based on a standard elec- tric typewriter. It provides the versatility and speed required, yet is smaller and less costly. The typewriter modifications needed for control of the operation, as well as to produce coded signals for recording, are described. The tape drive is powered from

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e typewriter and discrete tape movements e coupled to the typewriter carriage. A dif- ential spring mechanism for maintaining nsion on the coaxially mounted tape reels described. A circuit diagram is included hich emphasizes the fundamental sim- icity of the device.

M. M. Astrahan

55-109

Operating Experience with the Los amos 701—Willard G. Bouricius. (*Proc. stern Computer Conf., Joint IRE-AIEE-CM, December 8–10, 1953, Washington, . C.*, pp. 45–47; 1954). The operating poli- s of Los Alamos are described in some de- il. The system is self-service or "open op" in which customers code their own roblems. The group in charge of the ma- ine prepares utility programs and library broutines, provides computational consul- tion and conducts training programs. hree systems of coding are commonly em- oyed: Regional Coding, which is a method subdividing problems and coding them in mbolic machine language; Dual Coding, hich is an interpretive floating point ab- raction which permits easy switching be- veen the abstract and actual machine nguage; and SHACO (shorthand coding), hich is a three-address floating point ab- raction. Machine language coding ac- unts for approximately 65 per cent of the achine's time, Dual Coding 30 per cent, d SHACO 5 per cent. Usage of the 701 for e period April to October, 1953, is given as pproximately): Good time—80 per cent; heduled preventive maintenance time— per cent; Lost time due to machine and man error—5 per cent.

John R. Lowe

55-110

Experience on the Air Force UNIVAC—obert Kopp. (*Proc. Eastern Computer nf., Joint IRE-AIEE-ACM, December -10, 1953, Washington, D. C.*, pp. 62–66; 954.) The article discusses the Air Force xperience in developing a maintenance staff r the UNIVAC and in maintaining the achine. After about eight months' training y the manufacturer, a group of eleven men ndertook to operate and maintain the ma- ine on a 24-hour-per-day, 7-day-per-week asis. The writer notes in retrospect that this aff was considerably too small although in is opinion an adequate job was done under he circumstances. One of the serious prob- ms was adequate spare parts stocking. The riter recommends that a very complete tock be maintained at all times even though his is costly, since lack of a part may very ell cause complete shutdown of the ma- hine. Vacuum tubes accounted for a con- derable proportion of computer troubles. t was learned that one manufacturer's ubes were much superior to others. A com- on evidence of trouble was a G2-K short arying from 10,000 to 1,000,000 ohms. It is ypothesized that this trouble was occa- ioned by deposits of cathode material re- ulting from excessive heat within the ma- hine. Steps are being taken to improve this ondition by increasing the flow of cooling ir. The Scott transformer from three-phase o two-phase power burned out twice. A ommon and annoying trouble was blowing f grasshopper fuses which shuts down all dc supplies, sometimes resulting in blowing of diodes. The Uniservos represented a somewhat ticklish mechanical problem requiring considerable adjustment and the magnetic tapes sometimes caused trouble because of dirt, damage in shipping, breakage and wear. The performance of the machine from June, 1952, to December, 1953, was summarized as follows: Good time—61 per cent; Preventive Servicing—20 per cent; Down time—19 per cent. It is forecast that the good time will decrease due to wearing out of mechanical components and aging of diodes.

John R. Lowe

UTILIZATION OF DIGITAL EQUIPMENT

55-111

Use of Electrical Digital Computers in Optical Design—Gordon Black. (*Nature*, vol. 175, No. 4447, pp. 164–165; January 22, 1955.) This "Letter to the Editor" briefly outlines how the University of Manchester is using their computer for the automatic design of optical systems. The problem consists of minimizing a so-called performance function with respect to the variable constructional parameters of the system. The four principal machine minimization processes are iterative within themselves and with respect to each other. They are: (1) variable-by-variable minimization, (2) block relaxation, (3) group operations, and (4) random operations. A program using all these methods has been used and has improved lenses previously designed by other means.

D. E. Hart

55-112

The Automatic Analysis and Control of Computing Errors—Saul Gorn. (*Jour. Soc. Industrial and Applied Math.*, vol. 2, pp. 69–81; June, 1954.) Devices are considered by means of which a digital machine can be programmed to estimate the error entering into a computation and, in some instances, when the estimated error exceeds prescribed bounds, change the course of the computation to obviate this situation. Specific examples of the procedure are given in three cases: (1) systems of linear algebraic equations; (2) one algebraic or transcendental equation in one unknown; (3) systems of ordinary differential equations with initial conditions. The price to be paid for this additional feature in the computation, additional computing time, is considered worthwhile. The point is made that error-estimating routines can be coded to apply to any computational problem whatever.

Thomas H. Southard

ORIENTATION READING

55-113

Thinking Machines and the Human Personality—Elliot L. Gruenberg, (*Computers and Automation*, vol. 4, pp. 6–9; April, 1955.) The question is posed, "Are thinking machines a threat to the human personality?" Drawing on Hamlet, lines from a Broadway musical, and a quotation from Davidson, the author concludes that thinking is not a center of the personality and that thinking machines as a result are not a threat to it. The perennial question, "Can thinking machines be constructed?" is presented. The present discussion takes John Dewey's definition of the step of thinking. The author arbitrarily concludes that these steps can be performed by machine. He preserves the sanctity of the human personality by noting that Dewey's definition omits "goals" and that these must be supplied to any machine by humans.

Gordon Morrison

BOOK REVIEWS

55-114

Numerical Analysis—D. R. Hartree. (Oxford: Clarendon Press; London: Oxford University Press, xiv+288 pp.; 1952.) Prof. Hartree's book makes a considerable step forward in the literature of numerical analysis. The subject has a long history. It arose originally from the needs of navigators and astronomers and in the earlier days consisted largely of trigonometrical and geometrical applications. Later, calculations were aided by the invention and use of logarithms. Then elementary statistics was added, so that by the time the standard text-book of E. T. Whittaker and G. Robinson came to be written, an appropriate title appeared to be "The Calculus of Observations," in spite of the fact that a large proportion of the book deals with finite differences and other tools of the makers and users of mathematical tables. The Second World War greatly increased the demand for numerical work and stimulated the study of methods. In fact, numerical analysis is now recognized as a "respectable" subject for mathematical study. Thus, although "The Calculus of Observations" has been a standard textbook for several decades, and remains a scholarly and useful book, it was written in the early days when computing was done with logarithms or with the earliest barrel-type hand machines. It is consequently lacking in numerical illustrations and examples adequate to present-day needs. Other interesting and valuable books have also appeared from time to time, but they have either been too elementary to cover the most successful methods and formulae of modern numerical analysis, or they have been advanced and specialized mathematical textbooks on the theory of finite differences and difference equations. A further line of recent progress has been the rapid development of automatic electronic computers, with fantastic speeds of performance of elementary numerical operations. With their development, there has grown up a considerable body of users who have not had prior training in computing with desk machines, and who are unfamiliar with the many useful techniques that have been developed. There is thus a tendency to use simple, repetitive or iterative, but above all obvious, methods of computation on electronic machines and to argue that such methods are appropriate for such machines. There is, then, a clear need for a book for practical computers, whether working with desk or automatic machines, which will show them the kind of process which may or should be tackled numerically, which will tell them the best processes to use for carrying out the numerical work, and which will provide examples, both worked and unworked, to help them to attain a

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—*The Editor*

tter understanding of the processes described. Prof. Hartree's book meets all these eds. The aim of the book is practical, so at no attempt is made to cover ground yond practical needs, interesting though uch of this may be. For each process, the rmula or method advocated as best is ven in detail. Some further good methods e also described in case the author's choice ould not quite meet the user's needs. Very nsiderable emphsis is placed on the imrtance of *checking* and on methods for ing this. The derivation and use of finite fference formulas is covered thoroughly, th almost exclusive emphasis on the use of *ntral* differences, followed by chapters on terpolation, integration and differentiaon, and on the integration of ordinary and rtial differential equations. Linear and nlinear algebraic equations, and matrices, e covered fully, while a brief account is ven of methods for summation of series, rmonic analysis, and smoothing (with adeiate cautions on the often unappreciated ngers of this process). A final chapter on e organization of calculations for an autoatic machine gives an indication of possilities that will be more and more widerread in the future. This is a book that can recommended for all computers of all es—experienced or otherwise—and particarly as a text-book for students.

J. C. P. Miller

Courtesy of *Nature*

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Proceedings of the First Conference on aining Personnel for the Computing achine Field—Edited by Arvid W. cobson. (Wayne University Press, Detroit, ichigan, 104 pp.; 1955.) On an even hunred substantial pages, these attractively gotten up Proceedings give wide publicity to the tangled web of problems which, for years before, have been privately of much concern to the few who were in a position to foresee what demands the evolution of the computing machine field would inevitably place on this country's resources of trained personnel. The special care, given to the organization of the conference in view of its broad scope and significance, is reflected in the collection of printed papers and statements. Divided like the former into four sections, under the headings of (1) Manpower Requirements in the Computer Field; (2) Educational programs; (3) Influence of Automatic Computers on Technical and General Education; and (4) Cooperation Efforts for Training and Research; it touches on practically all the relevant aspects of the subject and its intricate relation to technical and industrial developments generally. Results of special surveys, made for the occasion, are reported by M. E. Mengel: "Present and Projected Computer Manpower Needs in Business and Industry"; by H. D. Huskey: "Status of University Educational Programs Relative to High-speed Computation"; by M. Kochen: "Implications of Automatic Computation for High School Training"; and by L. W. Cohen: "Cooperation between the National Science Foundation and Educational Institutions for Mathematical Research and Education." The following individual university programs are reviewed succinctly yet in adequate detail: Computer training at the University of Toronto; a graduate program in data processing at Harvard University; the undergraduate curriculum in machine-aided analysis at MIT; and, as an example of academic-industrial cooperation in the field, the Computation Laboratory at Wayne University. Similar treatment is given to the service training courses offered by Remington-Rand, the Electro Data Corporation, and General Electric. IBM, as well as government establishments like the Directorate of Statistical Services of U. S. Air Material Command, the Army's Ballistics Research Laboratory, and the Mathematics Division of the National Bureau of Standards are reported on staff composition, selection principles, and training activities. In addition, a great deal of experience and thought, long in maturing, has found its way on these pages into the public domain for the first time. In many respects a companion piece to the *Proceedings of a Conference on Training in Applied Mathematics* (Columbia University, October 1953), distributed by the National Science Foundation, the present volume does not attempt to formulate any principles of general agreement. It collects and ranges, rather than selects, the widely differing practices, policies, and ideas which have evolved in response to an equally wide variety of missions, environments, and philosophies. As such, it is addressed principally to the following three audiences: Staff members of schools and universities responsible for the education of students who might make their career in the computing machine field, students who contemplate such a career, and members of academic, industrial, or government organizations who have personnel responsibilities in connection with the maintenance and operation of a computer facility. All of them should find a thoughtful reading of this slim volume very rewarding. It wastes neither space nor words and stands as its own best summary.

F. Joachim Weyl

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—*The Editor*